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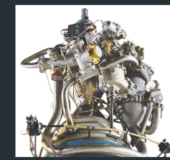
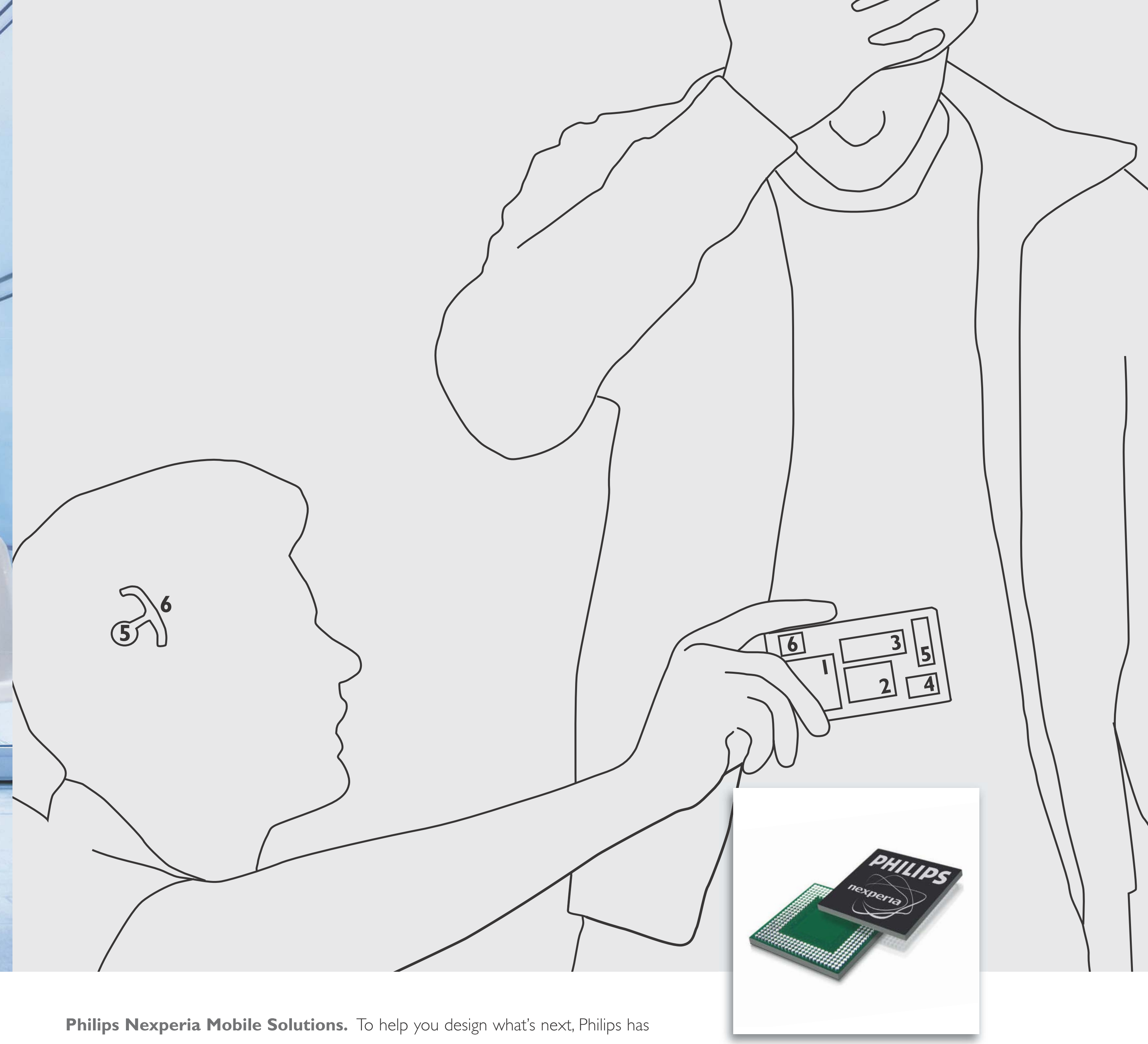


PROGRAMMABLE AUDIO PART ONE

FLEXIBLE SILICON: GUI-PROGRAMMABLE AUDIO PROCESSORS Page 60



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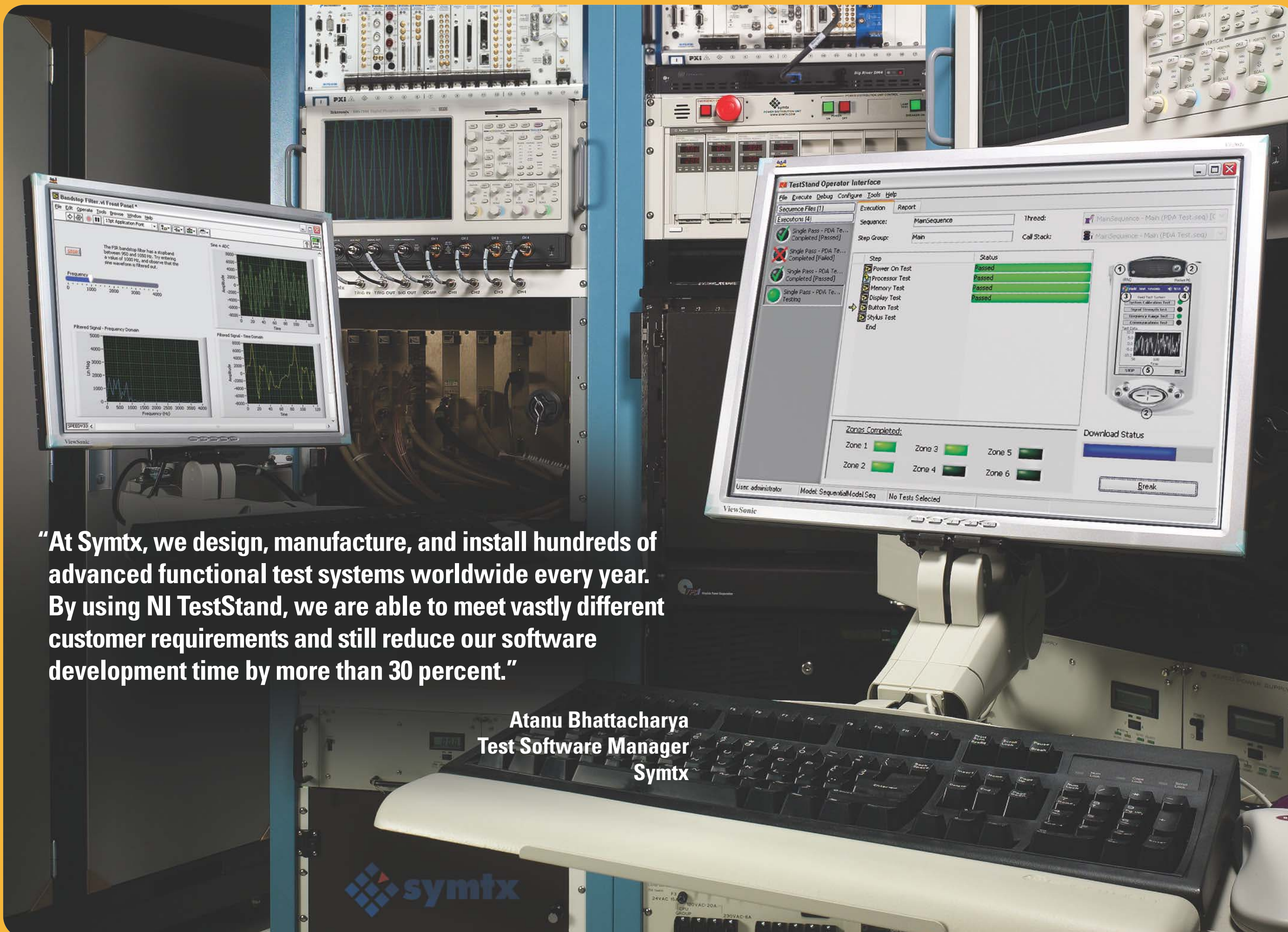

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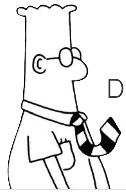

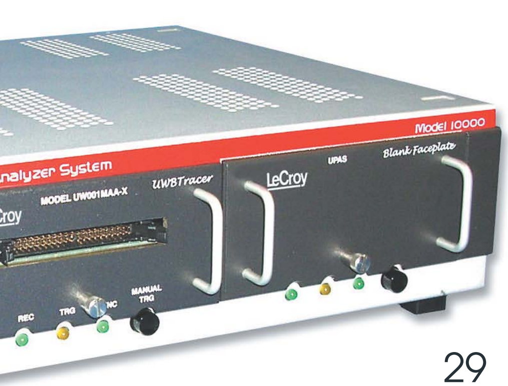

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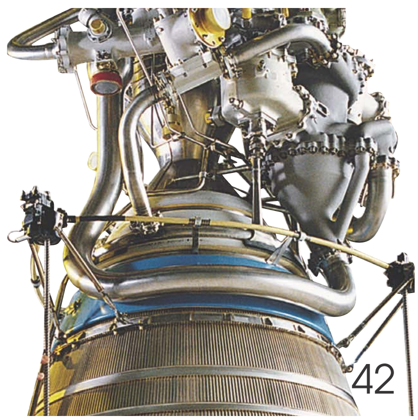
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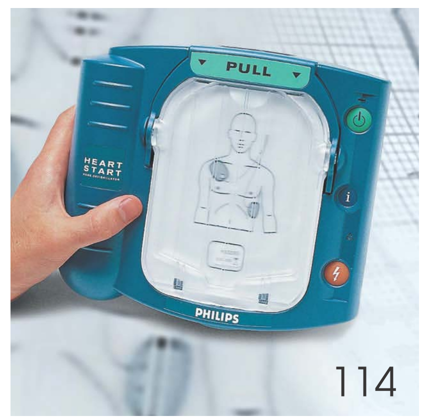

114

DEPARTMENTS & COLUMNS

PRODUCT ROUNDUP

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BY JOSHUA ISRAELSOHN, TECHNICAL EDITOR

What is a BenchPress?

Editor's note: *After much thought and effort, Joshua Israelsohn has produced our first BenchPress,* EDN's *term for a lab-based feature that looks well beyond the data sheet. Our goal is to provide designers yet more depth and dimension to* EDN's *unrivaled technical coverage. The BenchPress is also another reason that we proudly proclaim that* EDN *is the "voice of the engineer." Israelsohn's thinking behind the BenchPress follows.—John Dodge*

Most succinctly put, the BenchPress projects are a series of articles based upon instrumented measurements or observations. Their purpose is not to confirm or refute manufacturers' spec-table claims, but rather to examine products and their underlying technologies in a lab environment and to ask and answer questions that a product's data sheet may not fully address.

The BenchPress projects provide an opportunity for *EDN* technical editors to dig deeper into a technical topic than one can simply by relying on vendor-provided information, no matter how candid. They allow us to develop and report insights that are directly relevant to an OEM design engineer's information needs, concerns, and interests. The BenchPress projects take advantage of the fact that *EDN* technical editors are degreed electrical engineers with many years of design experience and a working familiarity with the wide range of products from which OEM designers draw.

Due to the high cost of instrumentation—a cost that rises dramatically with measurement bandwidth—BenchPress projects will most likely initially focus on narrow-bandwidth products, technologies, and applications in which measurement bandwidths less than 1 GHz suffice. The first such project, which appears as this issue's cover story, is a good example. In part one of "Flexible silicon: GUI-programmable audio processors," which begins on page 60, I begin to examine the traits of two high-level programmable audio devices and their design-support environments. This project would not have been possible without the support of Audio Precision Inc, which provided the core measurement capability in the form of the dual-domain, computer-controlled SYS-2722 audio analyzer. *EDN* would like to thank Audio Precision co-founder Bruce Hofer and President Alan Miksch for their generous support of the BenchPress projects. **EDN**

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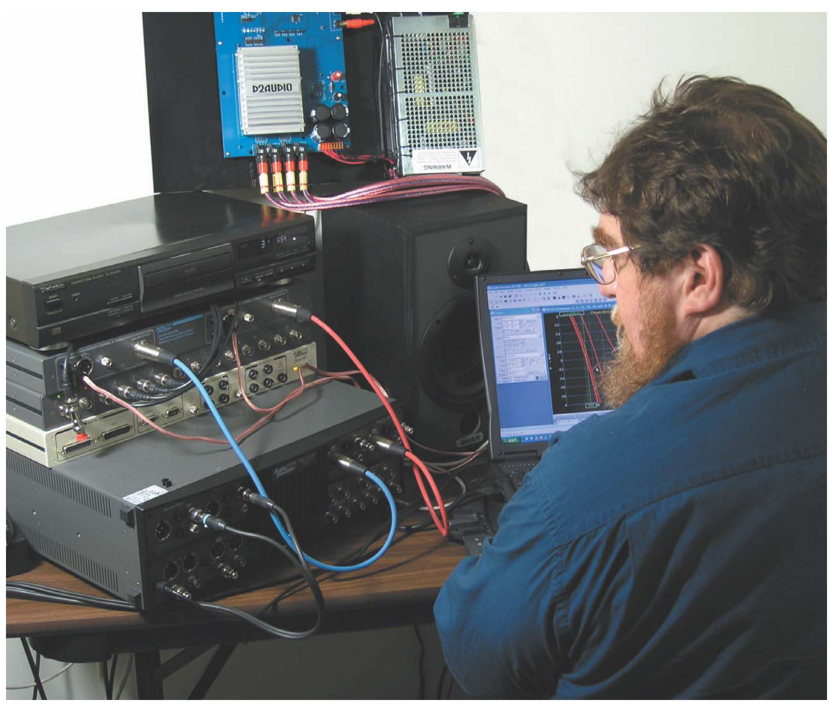

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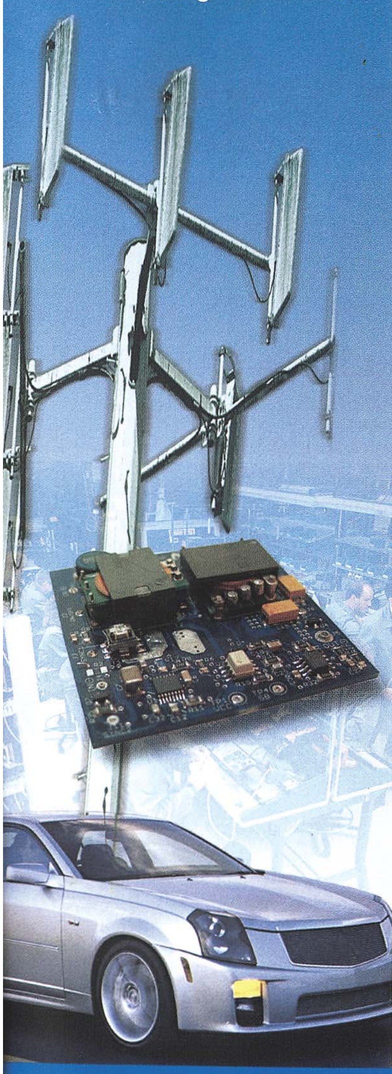

Operation and Benefits of Active-Clamp Forward Power Converters

— Bob Bell, Power Applications Engineer

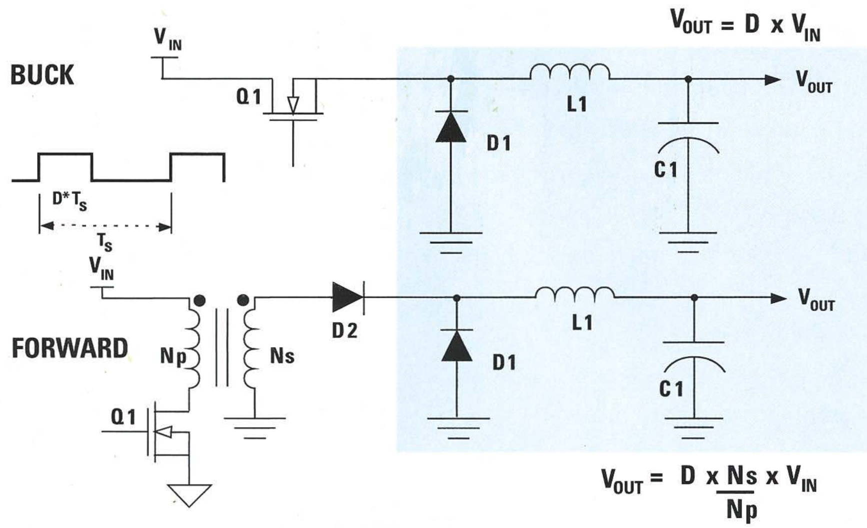

Figure 1. Buck and Forward Topologies

Forward converters with active-clamp reset offer multiple benefits to designers and are presently finding wide use. Power converters based on the forward topology are an excellent choice for applications where high efficiency and good power handling capability is required in the 50 to 500W power range. While the popularity of forward topology is based upon many factors, designers have been primarily drawn to it's simplicity, performance, and efficiency.

The forward converter is derived from the buck topology. The main difference between the two topologies is that the transformer employed in the forward topology provides input-output ground isolation as well as a step-down or step-up function. The transformer in a forward topology does not inherently reset each switching cycle as do symmetrical topologies (push-pull, half-bridge, and full-bridge). A number of different reset mechanisms have been employed in forward power converters, each method has its own benefits and challenges. Forward converters with active-clamp reset offer multiple benefits to designers and are presently finding wide use.

NEXT ISSUE:

Low-Power FPGA Designs

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100V Dual Interleaved Active-Clamp Current-Mode Controller

Highly Integrated LM5034 Maximizes Efficiency and Power Density of DC-DC Converters

Features

- Independent current-mode controllers
- Interleaved single or dual output operation
- Compound 2.5A main FET gate drivers
- Active clamp FET gate drivers
- Integrated 100V start-up regulator
- Up to 1 MHz switching frequency programmed by a single resistor
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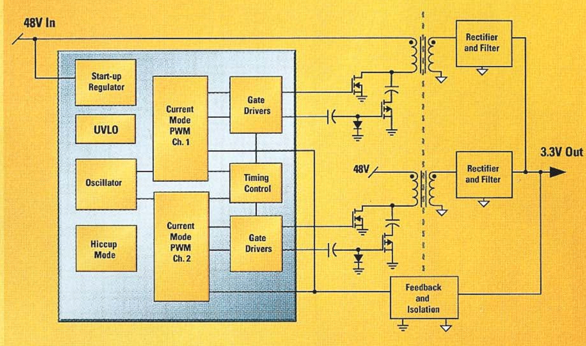
- Adjustable soft-start and input under-voltage sensing
- Adjustable deadtime between main and active clamp gate drivers
- Available in TSSOP-20 packaging

Ideal for telecom infrastructure, networking, industrial, and automotive power supplies

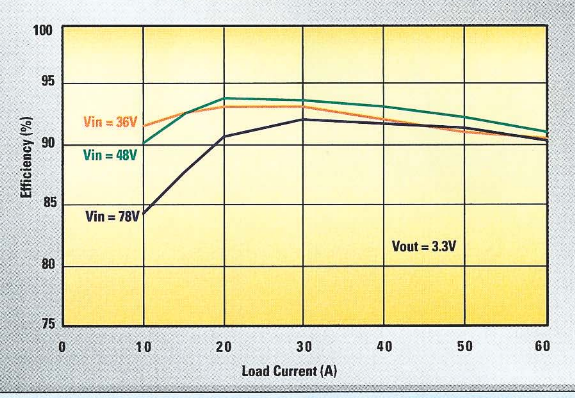
Product Highlight:

LM5034 enables high efficiency in 200W to 500W DC-DC converters while reducing input ripple

LM5034 Interleaved Forward Active Clamp Converter



LM5034 Efficiency Graph



Operation and Benefits of Active-Clamp Forward Power Converters

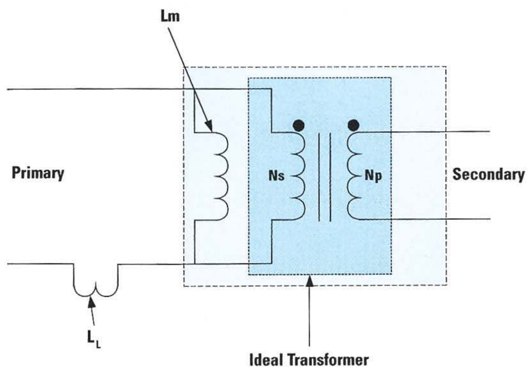


Figure 2. Transformer Model

Figure 1 shows the similarities between a buck and forward converter. Note the only difference between the transfer functions is the inclusion of the turns ratio term (Ns/Np) in the forward transfer function. Ns and Np are the number of secondary and primary turns, wound on the transformer core. *Figure 2* presents a transformer model, including the "Magnetizing Inductance" (Lm) shown in parallel with the primary winding. This magnetizing inductance can be measured at the primary terminals with the secondary winding(s) open circuit. The current in the magnetizing inductance is proportional to the flux density within the core. A given size core can only support a certain flux density before saturation of the core occurs. When the core saturates, there is a rapid reduction in inductance. Another element of the transformer model is the "Leakage Inductance" (L_L) in series with the primary winding. This leakage inductance can be measured at the primary terminals with the secondary winding(s) shorted. This term represents the stray primary inductance, which is not coupled to the secondary.

Active-Clamp Circuit Operation

Figures 3a through *3c* illustrate the main operational steps of an active clamp forward power converter. At time t0, the main power switch (Q1) is on, applying V_{IN} across the transformer primary. The transformer secondary winding voltage is V_{IN} x Ns/Np. The primary current is comprised of two components at this time; the reflected current from the output inductor (I_L x Ns/Np) and the current ramping up in the magnetizing inductance (Lm). The reset switch Q2 is open and the clamp capacitor (Cc) has been previously charged to a voltage of $V_{IN}/(1\text{-}D)$, which will be explained later. This interval is the power phase, energy is transferred from the primary to the secondary during this period. The approximate duration of the power phase is Ts x V_{OUT} / V_{IN}, where Ts is the switching period.

At time t1, the main power switch (Q1) is turned off and the reset switch (Q2) is turned on. The magnetizing current flows through the clamp capacitor and Q2 instead of through Q1. Since the clamp capacitor voltage is greater than V_{IN}, the voltage across the transformer primary is now reversed, compared to the power phase t0. Because the potential across the magnetizing inductance has been reversed, the magnitude of the magnetizing current will decrease as the energy stored in the

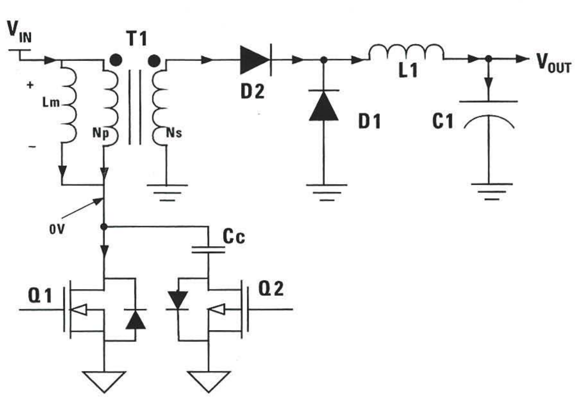


Figure 3a. Operation at Step t0

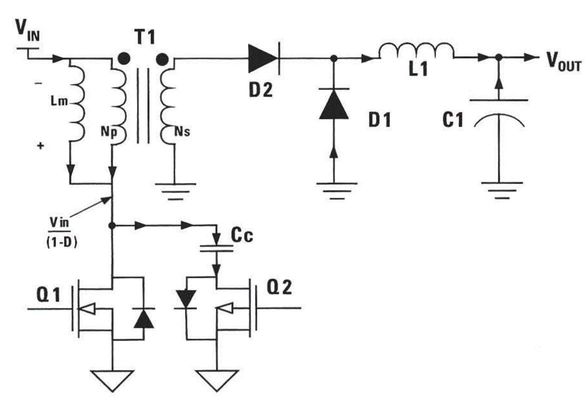


Figure 3b. Operation at Step t1

Current-Mode Controller for Forward Converters with Active-Clamp Reset

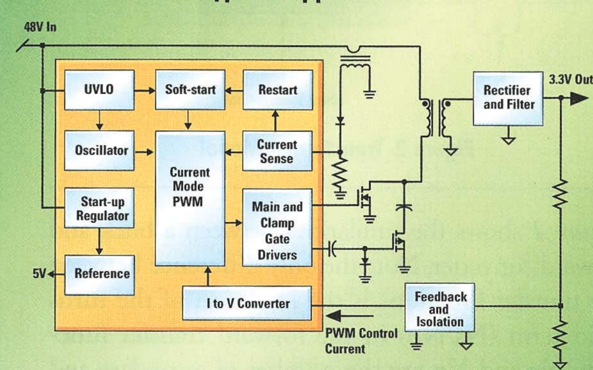
LM5026 Offers Versatile Dual-Mode Over-Current Protection with Hiccup Delay Timer

Features

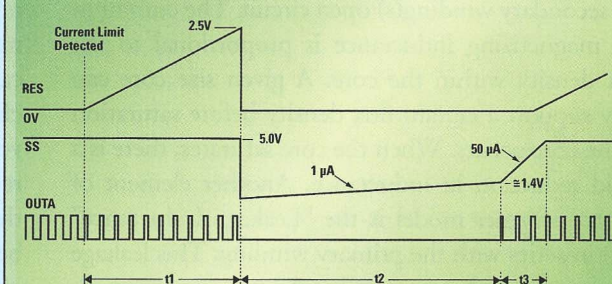
- Wide range (8V to 100V) start-up bias regulator
- Two high-speed power MOSFET drivers: 3A main output driver and 1A clamp driver
- User-programmable maximum duty-cycle and UVLO hysteresis thresholds
- User-programmable gate driver overlap and dead-time
- Versatile dual-mode over-current protection with hiccup mode delay timer
- TSSOP-16 or thermally enhanced LLP-16 packaging

Ideal for use in telecommunications power systems, +42V automotive power systems, -48V distributed power systems, industrial power supplies, and multi-output power supplies

LM5026 Typical Application Circuit

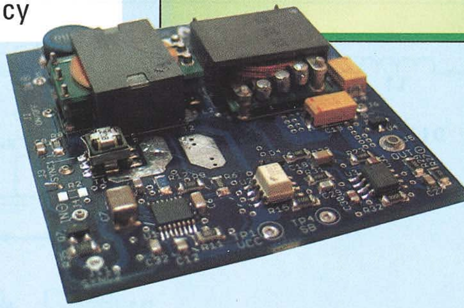


Hiccup Over-Load Restart Timing



Product Highlight:

Robust and flexible forward active-clamp controller offers highest efficiency



Operation and Benefits of Active-Clamp Forward Power Converters

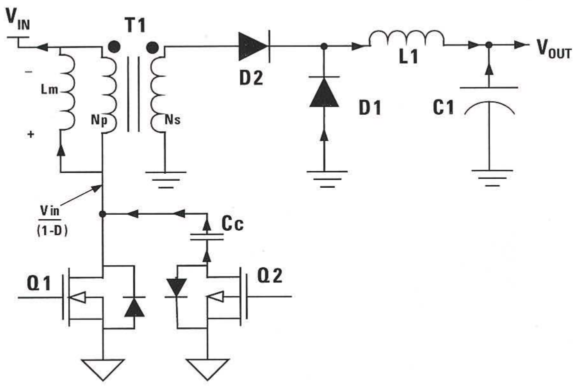


Figure 3c. Operation at Step t2

magnetizing inductance is transferred into the clamp capacitor. The voltage across the clamp capacitor increases slightly during this period and peaks when the magnetizing current reaches zero.

At t2, the current in the magnetizing inductance reaches zero and starts to build in the opposite direction, sourced from the clamp capacitor through the reset switch (Q2) and the magnetizing inductance (Lm) then back to the source (V_{IN}). The current will continue to build in the opposite direction as the clamp capacitor returns the energy that it had previously captured from the magnetizing inductance. Steady state conditions require the clamp capacitor voltage to return to the starting potential and the magnetizing current at the conclusion of the reset time to reach the same magnitude (opposite polarity) as the current at the beginning of this reset time. At the conclusion of t2, the switching period is over, as defined by the controller oscillator period. The reset switch is turned off, stopping the flow of current from the clamp capacitor.

Figure 4 shows several of the key circuit waveforms. The uppermost waveforms are the modulator ramp and error signals which determine the main switch on-time. The center waveform is the main switch drain voltage, which is low when the switch is on and rises to the clamp capacitor potential when the

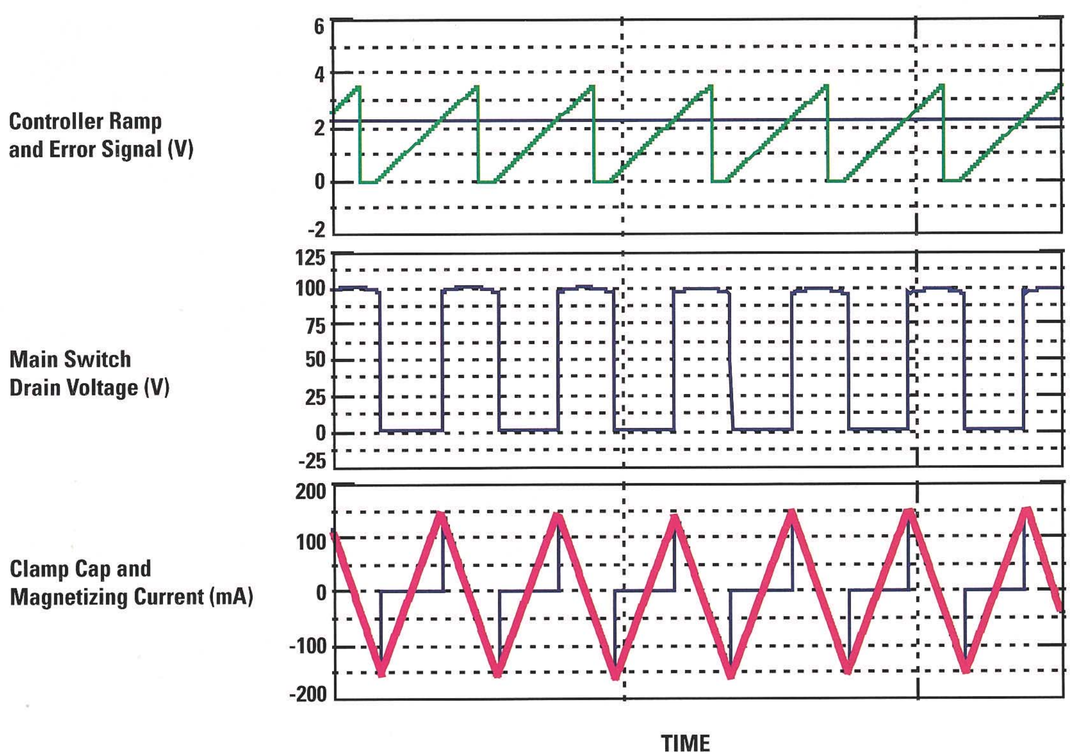
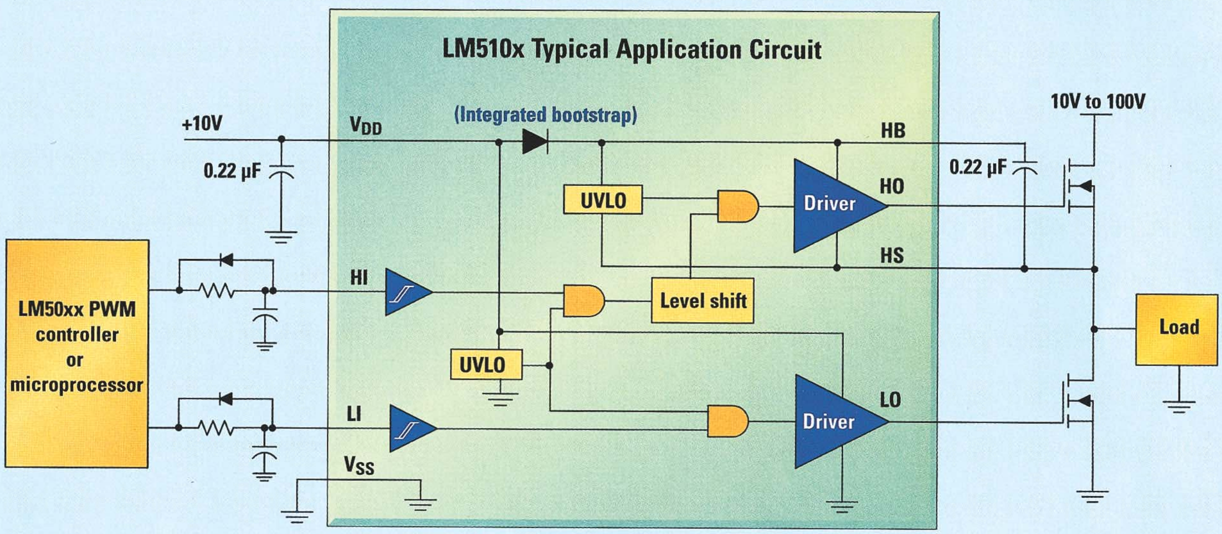


Figure 4. Key Active-Clamp Waveforms

100V Half-Bridge Power MOSFET Drivers

LM510x Family Offers the Industry's Highest Peak Gate Drive Current



Features

- Flexible configurations: interleaved forward, cascaded push-pull, half-bridge or full-bridge
- User-programmable turn-on edge delay feature (LM5105)
- New high-voltage bootstrap diode
- Best-in-class speed and efficiency in high-frequency switching regulator applications
- Negative load voltage transient capability down to –5V (LM5105/07)
- Available in SOIC and tiny, thermally enhanced LLP® packaging

Ideal for half-bridge and full-bridge power DC-DC converters, cascading current-fed or voltage-fed DC-DC converters, high-voltage buck DC-DC converters, and solid-state motor and solenoid drivers

Family Highlight:

Synchronous gate drivers optimized for every topology and high efficiency

Peak Gate Current	Product ID	Input Threshold	Packaging	Comments
NEW! 3.0A	**LM5100A/01A**	CMOS / TTL	LLP-10, SOIC-8	Upgrade on HIP2100/01
NEW! 1.8A	**LM5105**	TTL	LLP-10	Programmable dead-time, negative V_{LOAD}
NEW! 1.4A	**LM5107**	TTL	LLP-8, SOIC-8	Upgrade of ISL6700, negative V_{LOAD}

Operation and Benefits of Active-Clamp Forward Power Converters

switch is off. The red line in the lower waveform represents the magnetizing inductance current, which flows through the clamp capacitor (blue line waveform) during the reset time. As expected, both currents are balanced around the zero.

Benefits of Active-Clamp Reset

Several switching loss benefits can be realized with active-clamp reset. With sufficiently fast gate drive, the turn off of Q1 can be virtually lossless. To accomplish this, the gate of Q1 must be turned off (and the flow of current stopped) before the drain voltage has a chance to rise. The rise of the drain voltage is delayed due to the drain-source capacitance; a robust gate driver can turn off Q1 before the drain voltage increases significantly. The use of a compound gate driver made up of MOS and Bipolar devices provides a high peak gate discharge current to ensure a fast turn off and reduced switching losses. Turn-on losses can be reduced with proper selection of the switch delays, allowing time for the drain voltage reduction prior to the initiation of the main switch.

For steady state operation, the net Voltage x Time product applied to the magnetizing inductance over a complete cycle must equal zero. When the main switch is on, the Volt x Time product is $V_{IN} \times D \times Ts$, where D is the on-time duty cycle and Ts is the switching period. The off period is defined as (1-D) x Ts. The voltage across the primary when the main switch is off is $V_C - V_{IN}$, where V_C is the clamp capacitor voltage. In steady state operation, the Volt x Time products must be equal:

$$V_{IN} \times D \times Ts = (V_C - V_{IN}) \times (1-D) \times Ts$$

Solving for clamp capacitor voltage yields:

$$V_C = V_{IN} / (1-D)$$

Remember that the duty cycle (D) decreases as V_{IN} increases. The clamp capacitor voltage will adapt to changing line (V_{IN}) conditions to maintain this equality. This important feature minimizes the voltage stress across the main switch for all operating conditions, thus allowing use of lower $V_{(BR)DSS}$ rated devices. A lower MOSFET $V_{(BR)DSS}$ rating leads to lower on resistance and lower gate charge, which translates into higher conversion efficiency.

The energy stored in the leakage inductance is re-circulated rather than dissipated and the possibility of duty cycles over 50% leads to lower voltage stress on the rectifiers, further reducing losses.

Evaluation Boards

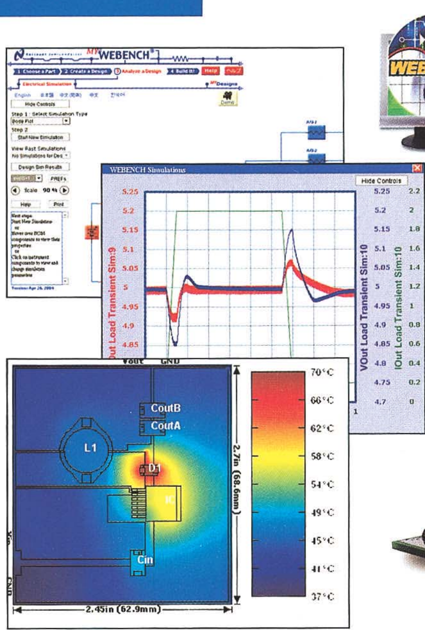
Several DC-DC converter demonstration boards employing active clamp reset are available, implemented with either voltage-mode or current-mode control. The input voltage range is 36V to 75V, with the output rated for 100W at 3.3V. The peak efficiency of 93% was measured at 15A load. The power transformer has a 6-to-1 turns ratio. The primary winding is made of 12 turns and the secondary winding is made of 2 turns. A planar construction technique is employed and the primary is fabricated with a multi-layer PC board. The high-current secondary is fabricated with insulated copper stampings.

The LM5025, LM5026, and LM5034 controllers directly drive the N-Channel power switch and a P-Channel reset switch. The internal gate drivers are sized differently for each switch. The reset switch only carries the magnetizing current allowing smaller gate drive. The main switch requires a robust gate drive in order to achieve the reduction in switching losses. The necessary timing delay between each of the gate driver outputs is programmable within the controller. The output rectifiers are implemented with synchronous MOSFETs. The active reset scheme eases the implementation of synchronous rectifiers as they can be self-driven.

Conclusion

In summary, the active-clamp technique allows the use of lower voltage rated MOSFETs and eases the use of self-driven synchronous rectifiers. The magnetizing and leakage energies are recycled and returned to the source. These benefits allow power converter designers to extend the power conversion efficiency. ■

Power Design Tools



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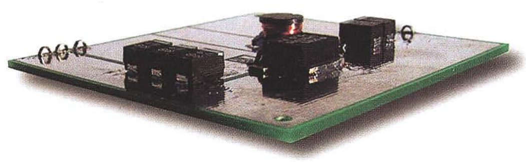

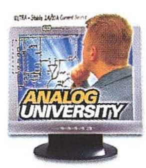

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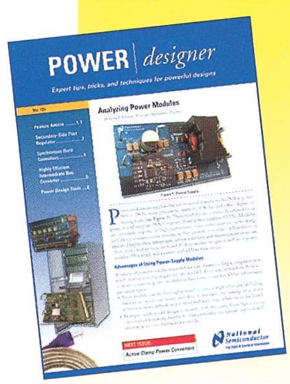

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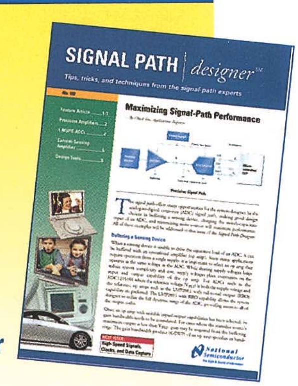

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pulse

INNOVATIONS & INNOVATORS

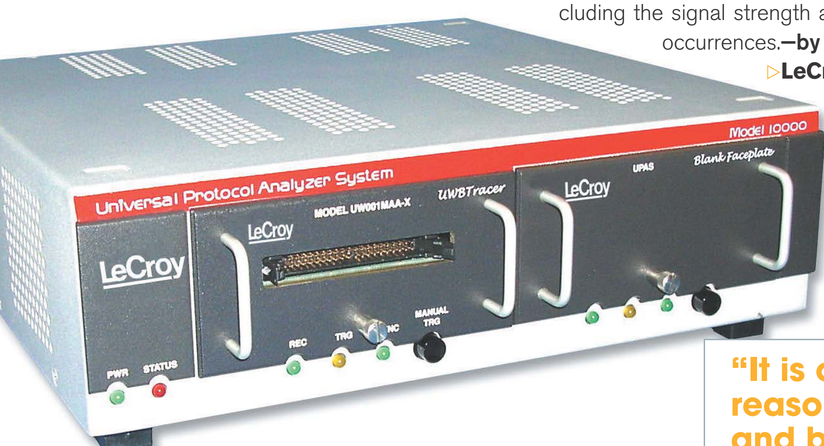
Protocol analyzer captures traffic between wireless USB MAC and PHY layers

The UWB (ultrawideband) Tracer MPI system helps design engineers solve problems with MAC/PHY (media-access-control/physical)-layer integration and interoperability in WUSB (wireless-USB) systems based on the USB-IF (USB Implementers' Forum) Certified Wireless USB 1.0 standard. The Forum based the standard on the WiMedia Alliance's MB-OFDM (multiband orthogonal-frequency-division multiplexing) UWB shared-bandwidth, short-range wireless-communication proposal. The USB-IF expects Certified WUSB to ultimately deliver data rates of approximately 1 Gbps at distances as great as 20m.

LeCroy Corp's Protocol Solutions Group designed the analyzer. LeCroy formed the group when the company acquired CATC (Computer Access Technology Corp) in the fall of 2004. According to James Wright, director of marketing for the group, CATC provided the first protocol analyzers for both USB and Bluetooth. "This new instrument captures and decodes at both the WiMedia and the WUSB levels," he says. By acquiring the traffic between the MAC and the PHY layers, it can display protocol traffic from systems during the design phase.

The $55,000 system uses the same Tracer-software structure that Wright says has become the industry's de facto standard for USB-protocol analysis. "By using the CATC Trace display," he says, "engineers can organize and display the protocol hierarchically at the WiMedia and WUSB levels. The software also includes pop-up tool tips, which provide information about the specifications, including packet structure and field usage." The instrument also displays real-time statistics, which provide information on the performance and operation of the unit under test, including the signal strength and number of frame occurrences.**—by Dan Strassberg**

▷**LeCroy Corp**, www.lecroy.com.

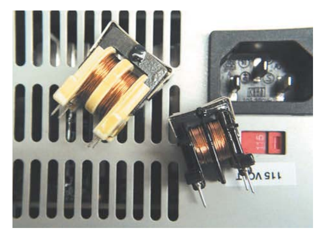


The UWB Tracer MPI, which captures and decodes at both the WiMedia and the wireless-USB levels, acquires traffic between the Certified Wireless USB MAC and PHY layers.

COMMON-MODE INDUCTORS CHOKE OFF CONDUCTIVE EMI

New through-hole inductors from JW Miller Magnetics put high inductance into a small footprint, most commonly for use as part of a line filter that suppresses conductive EMI from switched-mode power supplies. Devices in the Model 7400 family measure 19×21 mm; inductance ranges from 0.6 to 45 mH, and dc resistance is 0.025 to 2.68Ω. Operating temperature is −55 to +105°C for these approximately $1 units.**—by Bill Schweber**

▷**JW Miller Magnetics**, www.jwmiller.com.



The Model 7400 inductors provide effective common-mode inductance in a small, through-hole package and suppress power-supply EMI.

"It is one thing to advocate—perfectly reasonably—for free-market principles and by extension allow a foreign company to purchase a US company. It is quite another to allow an—often hostile—foreign government to purchase the resources of a US company."

Mark Boyles, in *EDN*'s Feedback Loop at www.edn.com/article/CA629313. Add your comments.

Control-networking technology delivers smaller, cheaper nodes

Echelon, the developer of the LON (local operating network) sold under the LonWorks brand, now has a new technology, Pyxos, that the company claims will be cheap enough to connect sensors and actuators in everyday equipment. Designers have commonly used LonWorks products to automate building control in lighting, HVAC, security, and other systems. But generally, LonWorks would prove too expensive to use in a control network within a product such as an air conditioner or a spa controller. Echelon believes that Pyxos will bring connectivity into such systems.

The benefits include simpler design because a low-cost, free-topology wiring system can connect sensors and actuators in place of traditional wiring harnesses—a benefit similar to what CAN (controller-area-network) technology brings to the automobile. A Pyxos-enabled appliance could also allow a user to perhaps use a cell phone to remotely control a device such as a spa. And manufacturers could enable preventive maintenance on Pyxos-enabled products. Alas, Pyxos doesn't seem to offer much toward a truly automated home for the broad consumer base because the cheapest Pyxos chips will still sell in the $2 to $3 range in low volumes.

From a software perspective, a Pyxos node can operate just as a LonWorks node, and designers can link subnetworks of as many as 32 Pyxos nodes to a LonWorks network through an access point. Alternatively, a designer could use Pyxos chips alone in a network without LonWorks. The Pyxos nodes share the transceiver technology in LonWorks, including RF, power-line, and twisted-pair technology. Twisted-pair cable can carry both the data signal and the power to Pyxos nodes. And designers can connect Pyxos nodes in bus, star, and loop topologies.

In its simplest form, a Pyxos node requires only a Pyxos chip, a transceiver, and the connection to a sensor or an actuator. The baseline Pyxos chip includes digital I/O to connect to simple sensors and actuators and needs no on-board microcontroller. Instead, vendors can preconfigure Pyxos chips at the factory, and the nodes self-install themselves into workable networks. More complex nodes might include a microcontroller, data converters, and LonWorks links.

Echelon claims that, together with partners, it has deployed more than 50 million LonWorks control devices. Company Chairman Kenneth Oshman projects that the potential Pyxos market is two orders of magnitude greater than the LonWorks market. The company predicts scenarios as wild as a smart carpet that can track traffic patterns so that cleaning crews concentrate on busy areas.

—by Maury Wright

▷**Echelon Corp**, www.echelon.com.

FEEDBACK LOOP

"Unless NASA has something better to offer, I would rather spend the money on a booster for our kids' education than a booster rocket to launch a space mission of dubious importance."

Michael Potash, in *EDN*'s Feedback Loop at www.edn.com/article/CA632662. Add your comments.

DILBERT *By Scott Adams*

09.29.05

SAW duplexer cuts weight by shifting to plastic package

Every milligram counts in today's portable-system world; new SAW (surface-acoustic wave) duplexers from NDK (Nihon Dempa Kogyo) make this point by switching from ceramic to plastic packages and cutting weight by 40 to 50%. The WX807C, for US CDMA application, has a nominal transmitter-band center frequency of 836.5 MHz and a receiver-band frequency of 881.5 MHz. The similar WX910A for UMTS applications has transmitter and receiver frequencies of 1950 and 2140 MHz, respectively.

Maximum insertion loss for these duplexers is just 2 dB in the transmitting path and 2.8 dB in the receiving path, with attenuation of 43 and 55 dB, respectively. The 50Ω duplexers measure 3.8 mm sq and 1.5 mm high. The CDMA WX807C sells for $1.15, and the UMTS WX910A sells for $1.62 (10,000).

—by Bill Schweber

▶**NDK America, www.ndk.com.**

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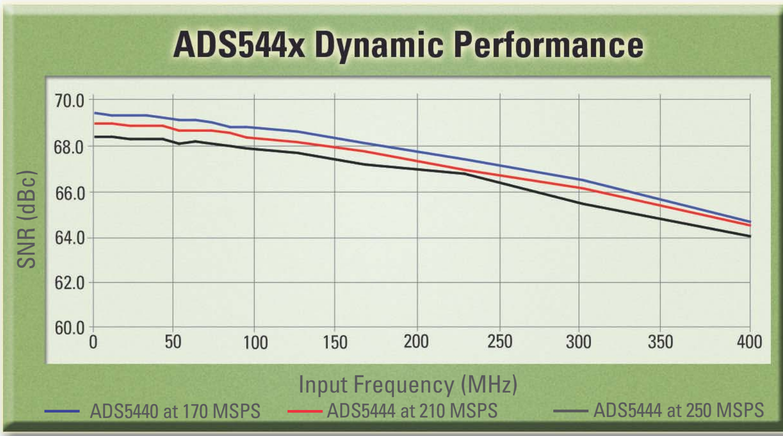
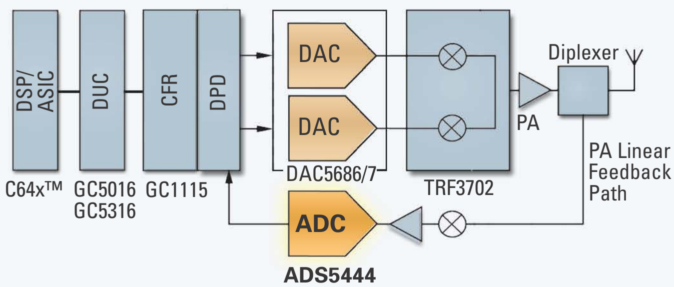


Sample Application: Wideband, High IF DPD Feedback Receiver



The new **ADS5444** from Texas Instruments sets a new benchmark for high-speed ADCs, providing best-in-class performance at 250 MHz. Look to TI for a complete portfolio of high-speed ADCs, including the recently announced ADS5440 13-bit, 250 MSPS ADC.

Device	Resolution (Bits)	Speed (MSPS)	SNR (dBc)	SFDR (dBc)
ADS5444	13	250	68 at 230 MHz IF	75 at 230 MHz IF
ADS5440	13	210	68 at 230 MHz IF	79 at 230 MHz IF
ADS5500	14	125	69.5 at 100 MHz IF	82 at 100 MHz IF
ADS5424	14	105	74 at 50 MHz IF	93 at 50 MHz IF
ADS5541	14	105	71 at 100 MHz IF	86 at 100 MHz IF
ADS5423	14	80	74 at 50 MHz IF	94 at 50 MHz IF
ADS5520	12	125	68.7 at 100 MHz IF	82 at 100 MHz IF
ADS5521	12	105	69 at 100 MHz IF	86 at 100 MHz IF

▶ Applications

- Software-defined radio
- Base stations:
  - Wideband receiver
  - High IF receiver
  - PA linearization
- Instrumentation
- Test and Measurement

▶ Features

- 100 MHz IF: SNR = 68.7 dBc; SFDR = 73 dBc
- 230 MHz IF: SNR = 68 dBc; SFDR = 75 dBc
- Fully buffered analog inputs
- 2.2 Vpp differential input voltage
- 3.3 V LVDS compatible outputs
- TQFP-80 PowerPAD™ package
- Industrial temperature range –40°C to +85°C
- Price: $95 1k

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FPGAs become rad-tolerant, rad-hard

Actel recently unveiled the latest device in its radiation-tolerant FPGA family and also announced that it is working on its first fully radiation-hardened FPGAs. The new RTAX4000S radiation-tolerant FPGA has twice the gate count of the company's last rad-tolerant FPGA, the RTAX-S, according to Ken O'Neill, director of military- and aerospace-product marketing. The new device, which has 500,000 ASIC gates, 840 I/Os, and 540 kbits of embedded memory, suits space applications, such as satellite-payload systems and scientific satellites.

Actel has built the device to the same radiation-tolerance standards as its other RTAX-S devices, O'Neill says. The FPGA includes embedded RAM with EDAC (error detection and correction), flip-flops that are practically immune to SEUs (single-event upsets), and memory-upset levels of less than 1^{-10} errors/bit/day.

The devices are immune to configuration upsets and have a TID (total-ionizing-dose) resistance as high as 300k rads (functional), which exceeds the requirement for most space applications and is more than ample for most space programs, according to O'Neill. Functional prototypes of the device, which aren't rad-tolerant, will be available in the first quarter of 2006, and radiation-tolerant versions will become available at the end of 2006.

In addition to the RTAX-4000S, Actel also announced that it is making progress in the development of its first radiation-hardened FPGAs, which take reliability one step beyond the radiation tolerance of its RTAX4000S. The upcoming RHAX-S family increases the reliability of the device to QML (qualified materials list) Class V. The projected device family will feature a TID resistance of 1M rad and logic and memory SEU resistance of less than 1^{-10} upset errors/bit/day.

The first device in the RHAX family will be a 250,000-system-gate (30,000-ASIC-gate) FPGA. Actel expects to deliver the prototype by the end of 2006 or early 2007 and production parts in 2008.

—by Michael Santarini

▷**Actel Inc**, www.actel.com.

Multimode RF transceiver targets WEDGE mobile handsets

09.29.05

As cellular standards evolve toward 3G and beyond, the range of frequency bands and modulation schemes continues to broaden. Handset designers want to support legacy networks and strive to integrate support for next-generation networks. In the GSM (global-system-for-mobile-communications) space, the current state-of-the-art target is WEDGE, which combines WCDMA (wideband CDMA) and EDGE (enhanced data rate for global evolution). The emerging WEDGE phones, however, often use a combination of RF front ends that are glued together to support the new WCDMA standard that will extend data rates to 2 Mbps, whereas EDGE supports 385-kbps rates.

Start-up Sequoia Communications claims to have a SiGe (silicon-germanium)-based transceiver design that can support the full range of GSM-centric standards, including GPRS (General Packet Radio Service), EDGE, and WCDMA.

Sequoia is entering a crowded field seeking a share in the transceiver market. Vice President of Marketing and Business Development Charlie Wilcoxson points out that, although the market is crowded, no player has a dominant share. Wilcoxson shows a pie chart in which no provider of transceivers in the GSM market has a 20% share. And Wilcoxson claims that Sequoia has a technology that the other competitors lack in the new SEQ-5400 chip.

Sequoia is demonstrating first silicon in the lab transmitting and receiving the full slate of cellular signals in frequency bands of 800 to 2100 MHz. The fully analog implementation also integrates a SAW (surface-acoustic-wave)-receiver filter that other dedicated WCDMA transceivers lack. The company claims that the design will take the RF footprint in a WEDGE phone from 15.2 cm^2 to less than 7 cm^2. Sequoia also claims to be the first company to use polar modulation in a WCDMA transceiver. Wilcoxson believes that most competitors realize the benefits in power efficiency of polar modulation but haven't figured out how to apply the technique in WCDMA designs and are therefore using less-efficient linear modulation.

Sequoia claims that its chip will reduce the BOM (bill-of-materials) cost of the RF components in a WEDGE handset by 40 to 60%. The RF BOM cost in such a phone is now probably approximately $20. Samples are available now with volume slated for the first half of 2006. You could argue that the product is ahead of the market, and WCDMA hasn't taken off in North America. But Wilcoxson claims shipments are ramping in Europe and Asia. The company will also face a challenge with its first product targeting such a cutthroat market. Moreover, the DSP-based software-defined radios are waiting in the wings to support multiple cellular standards and even WiFi (Wireless Fidelity) technology.

—by Maury Wright

▶**Sequoia Communications**, www.sequoiacommunications.com.

Beam-forming WLAN implementation targets audio/visual usage

The Ruckus Wireless MF2900 video-capable 802.11g access point and router features a six-element smart antenna in the upper half of the clamshell and dynamic software control that forms signal beams through 63 antenna patterns.

Yet another company has emerged with an approach to the problem of wirelessly moving digital audio and video around the home. Vendors have proffered one of the many standard or enhanced flavors of 802.11 or WiFi (Wireless Fidelity) WLAN (wireless-LAN) technology as cable replacements, but each has so far met insurmountable obstacles in data rate, range, or cost. The WLAN industry hopes to solve the problem with the 802.11n standard that the IEEE is now developing. Ruckus Wireless (formerly, Video54), meanwhile, claims that its beam-forming-antenna technology can now enable video distribution and later further extend the capabilities of 802.11n.

Ruckus is already shipping the technology in the Netgear RangeMax family of products. The company refers to its beam-forming technique as MIMO (multiple-input multiple-output), but it doesn't include the baseband-resident spatial multiplexing technology that first carried the MIMO label (see "The greed for speed," *EDN*, Feb 19, 2004, pg 26, www.edn.com/article/CA379885). Of late, companies that want to cash in on the popular MIMO label are using the term on any implementation with multiple antennas. Pioneer Airgo Networks has taken to labeling spatial-multiplexing technology as true MIMO, which the 802.11n standard will mandate. Still, the beam-forming offering from Ruckus does boost range, as well.

The latest Ruckus announcement combines the BeamFlex beam-forming capability with the SmartCast software stack that ensures quality of service for video streams. The company will license both technologies to OEMs, as it did BeamFlex to Netgear. And Ruckus will now supply access points and wireless adapters to service providers. The initial target customers are the major phone companies worldwide that are seeking to deliver IPTV (Internet Protocol television), or video over their phone lines. According to Michelle Abraham, an analyst with In-Stat, there were 1.6 million IPTV subscribers at the end of 2004, although In-Stat projects that market will grow to 32 million subscribers by the end of 2009.

IPTV schemes typically deliver video packets to a broadband modem/router that in turn must send packets to a set-top box in the living room. Most early players in IPTV are simply rolling trucks and installing Ethernet cables between routers and set-top boxes, but Ruckus believes it can make that connection wireless and user-installable. The company estimates pricing of $169 for the MF2900 access point/router and $129 for the MF2501 set-top adapter, although service providers could subsidize such gear.

Ruckus claims that its implementation supports greater range and is less sensitive to interference from nearby wireless networks or other noise sources, such as a microwave ovens. For service providers, the company is offering a product using six antennas in the access point. Software that controls the antenna operation adopts one of 63 antenna configurations for each wireless client and therefore sends a relatively narrow beam of energy that minimizes interference to nearby networks. Moreover, the ability to dynamically adapt signal paths through antenna patterns allows the receiver to adapt for interference. Along with announcing the Ruckus access point and adapter, the company also announced its first customer, PCCW, a Hong-Kong IPTV-service provider.

The Ruckus technology looks promising, although it will be more applicable once 802.11n and data rates in excess of 100 Mbps are prevalent. Ruckus claims it will extend range by two or three times even on those next-generation MIMO systems. Today, the company claims it can reliably support rates of 11 to 25 Mbps using 802.11g chips. It's unlikely that such a system could handle an HDTV stream, although Ruckus claims it can. A live, action-packed program, such as a football game, would need speed at the upper end of that range. And supporting multiple standard-definition streams could also be an issue. And, finally, so many WLAN-video approaches have failed coming to market that all new ones have questionable credibility.**—by Maury Wright**

▷**Ruckus Wireless**, www.ruckuswireless.com.

FEEDBACK LOOP

"If the moon were solid gold or if Mars were habitable and had new animals and plants to see, we would probably already be there. But, so far, everything we have found out there is just dirt and rocks, so it is hard to get the public excited."

Jim Harrison in *EDN*'s Feedback Loop at www.edn.com/article/CA632662. Add your comments.

RAQ's

Rarely Asked Questions

Strange but true stories from the call logs of Analog Devices

Isolating the Key Detail (or Lunching With a Mermaid and Pickled Herring)

Q. *There is a fault in my CMOS multiplexer . . .?*

A. Recently, we considered an applications problem where the engineer was reticent, making it difficult to obtain the facts needed to solve it. Long ago, just after I joined Analog Devices, I met a problem where all details but one were almost irrelevant.

It was in Copenhagen. I had been discussing an analog electronics course with a professor from the University of Copenhagen and we decided to walk through Kastellet to see the Little Mermaid on her rock before having lunch on the quayside at Nyhaven in the oldest part of the harbor. As we walked Lars told me that Karen, one of his graduate students, was having accuracy troubles making measurements on three channels with one analog-to-digital converter (ADC).

If there are three channels there is usually a fourth not being used—so I told him I could probably cure the problem on that information alone. We telephoned the student and told her to ground all unused multiplexer (MUX) inputs and outputs, and retest her system.

Unconnected channels on CMOS switches and MUXes, whether on a separate chip or part of a multi-input ADC, can pick up signals from stray electrostatic fields and inject them into the substrate of the chip, turning on spurious substrate devices—even if the unconnected channel is disabled. These devices' leakage can degrade the performance of the active channel or channels, or even of an ADC which shares the chip.

In the past the effect might be so large as to trigger a parasitic thyristor across the supplies and destroy the device, but modern CMOS processes are mostly protected against such catastrophes, but not against more subtle degradations of accuracy. "Fault-protected" switches and MUXes are far less vulnerable to such effects, too, but not totally immune—and by no means are all MUXes fault-protected as the protection circuitry increases chip size and, as a result, cost.

It is therefore essential that all inputs and outputs of a CMOS switch or MUX, even one integrated into an ADC, be connected to a potential somewhere between its supplies. Generally this means grounding all unused inputs and outputs, but sometimes leakage and/or capacitive crosstalk can better be minimized by connecting unused pins to a signal or a power supply.

By the time Lars and I had consumed a Tuborg and a plate of marinated herring, and had waved goodbye to the mermaid, Karen had called us back to report that her system was working perfectly.

To learn more about behavioral problems in ADCs & how to avoid them
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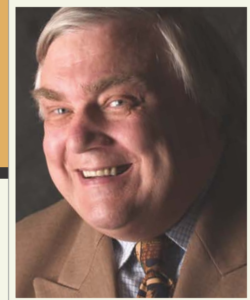

Contributing Writer James Bryant has been a European Applications Manager with Analog Devices since 1982. He holds a degree in Physics and Philosophy from the University of Leeds. He is also C.Eng., Eur.Eng., MIEE, and an FBIS. In addition to his passion for engineering, James is a radio ham and holds the call sign G4CLF.

Have a question involving a perplexing or unusual analog problem? Submit your question to:

raq@reedbusiness.com

Q&A

Power plays

Saul Kupferberg, vice president of sales at power-supply vendor Kepco Inc

Saul Kupferberg is a second-generation member of the founding family of Kepco, which brothers Jack, Jesse, Max, and Ken Kupferberg founded in 1946. The company grew out of the involvement of three of the four founders in one of World War II's "Big Science" projects—the Manhattan Project. Much of the work they did at Los Alamos remains classified to this day. The work they were involved with required them to help invent and build electronic instruments. They had to build their own instruments because there really were no electronics businesses and no commercially available electronic instruments at that time. Indeed, the word "electronic" had not yet been coined.

Where do users of products such as yours have the greatest misunderstandings?

A People get confused on how to use remote error sensing to compensate for voltage drops. We always find we are re-educating engineers about it. We even publish a nomograph of how to size the wires for the situation. It usually starts with a call from someone saying "Your power supply is not working."

What's your impression of the state of engineering and science education?

A We find that US-educated engineers and others give little attention to analog and power design. Engineering graduates looking for work have never had a hands-on components or circuits experience or ever debugged a circuit. That's a big problem for our own talent needs and for our customers. The course they take has been simulation only. The general level of education is good, but the courses haven't focused on these aspects. In Europe, the analog-design and hands-on-experience portion of education is stronger.

What changes in specifications have you seen?

A Switching supplies have become more and more dominant, combining low noise, a rise in PFC [power-factor correction], and harmonics regulation. Increasingly, we have to provide switching supplies that meet both conducted- and radiated-noise specifications. We saw the first switchers with PFC about 10 years ago. Now, everything above 50W has PFC and must meet the conducted- and radiated-emissions standards. Aerospace, sensor testing, and sensitive applications still need linear supplies.

Do you find that customers are increasingly asking you to do more?

A Customers are asking us to do more of their work for them, especially in software applications. We want to help them, but at what point do we cross the line and are doing their job, as consultants? And helping them to this extent means there are other customers we can't help.

Why does the power-supply industry have so many vendors?

A About 60 to 75% of the market is custom, so there are always those who do a custom unit and then hope to sell it as a standard product. Also, everybody thinks they can make a power supply, and, to some extent, it's true. It's make-versus-buy: They can make one, but can they make it over and over? It's an opportunity for companies such as ours. It takes a lot of time and energy to purchase components, and then you have to spend money to get past UL and other approvals. The BOM [bill-of-materials] cost is less than buying from us or others, but the total cost is not. There are so many hidden costs and other things that you could be doing with your engineering time. Lots of good engineers can build one supply, but to build tens or hundreds—that's another story.

Have any incidents caused a chuckle?

A I was at a prestigious educational institution where we had delivered three 0 to 20V, 0 to 20A supplies. The postdoctoral student couldn't understand why he couldn't get 0 to 60V, 0 to 60A from the supply trio at the same time. I had to politely explain to him that he could connect them in series for the higher voltage or in parallel for the higher current—but not at the same time.

–by Bill Schweber

FEEDBACK LOOP

"The ability to see, to know, and to say are crucial to our modern lifestyle and sense of freedom. However, it is our power to *do* that makes for change. At least once a season since the late 1980s, hurricane victims directly benefit from the application of convenient, cordless power tools."

Chris Walter, in *EDN*'s Feedback Loop at www.edn.com/article/CA607116. Add your comments.

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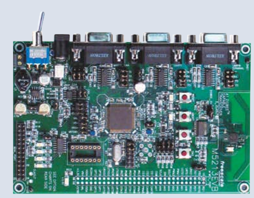

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Memory	Up to 256K bytes interleaved flash	SDR/DDR/Mobile-DDR SDRAM Controller
Power Management	Distributed clocking, stop/wait/doze modes, and bypass features	

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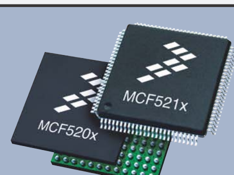

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GLOBAL DESIGNER

DVD-recorder processor targets European digital-broadcast reception

LSI Logic recently unveiled a single-chip DVD-recorder-processor platform, which, it claims, reduces system costs to support digital-broadcast reception in Europe and other parts of the world. The company also claims that the device will enable consumer-electronics vendors to design set-top-box/DVD recorders and set-top-box/hard-disk-drive/DVD recorders. According to technology-research company In-Stat, there are approximately 9.5 million digital-television subscribers in England, Germany, France, Italy, and Scandinavia. "This brings the benefits of a combined set-top-box/DVD-recorder platform to the home and is gaining momentum in Europe," says Vijendra Kuroodi, LSI senior product manager for DVD-recorder products.

The new offerings include the DMN-8623 and DMN-8673 single-chip processors, which the company based on its proprietary DoMiNo architecture, comprising hardware and programmable software. Both of these processors integrate set-top-box-receiving and DVD-recording functions on one chip. "A single-chip approach eliminates a lot of redundancies for consumers and designers," says Kuroodi. Chief among these redundancies are memory systems, MPEG decoders, host processors, and graphics engines, all of which significantly reduce the bill-of-materials costs.

The DMN-8623 targets use in single-drive DVD recorders and can record and play back a digital-TV channel or video stream. The device has a single optical drive with a DVD-recorder-drive interface that enables digital downstream access. The DMN-8673 focuses on hard-disk-drive/DVD-recorder systems that can encode or decode two digital- or analog-TV streams, which users can record onto a hard drive or DVD in a manner similar to using TiVo.

"The DMN-8673 can connect to a hard-disk drive and enables you to time-shift live content more than an optical disk can, as well as make backup recordings, which you can view later," says Kuroodi. "It can simultaneously process two video inputs by encoding video on a hard disk and then decoding it onto the display." The DMN-8623 and DMN-8673 are available for sampling and cost $25 and $30, respectively (high volumes).

—by Jeff Berman

▷**LSI Logic**, www.lsilogic.com.

The DMN-8623 and 8673 chips integrate set-top-box and DVD functions.

09.29.05

CSIA employs VSIA standards

The VSIA (Virtual Socket Interface Alliance), a SIP (semiconductor-intellectual-property) standards group focusing on design reuse, and the CSIA (China Semiconductor Industry Association) recently inked a deal in which the CSIA will base its SIP standards on VSIA's standards. This arrangement will let the CSIA develop standards in Chinese, leveraging VSIA standards, which the CSIA will distribute throughout China. "This is a major change for China as it pushes to have standards driven by commercial interest [through a combination of companies and universities] and directly through the government," says Larry Rosenberg, VSIA vice president of engineering. "China wants to have standards that are compatible with the rest of the world."

The organizations will also charter a Chinese VSIA SIG (special-interest group), which provides limited access of VSIA standards to a group of 35 Chinese companies, each with annual revenues of less than $10 million. The group will focus on ways of integrating IP into SOCs (systems on chips) and on IP protection.

A major factor in the CSIA's decision to collaborate with the VSIA and obtain legal rights to create a Chinese derivative of VSIA standards was that the CSIA wanted to change how China acts in IP protection and how the rest of the world perceives the country. Rosenberg notes that officially licensing IP is a significant step toward those goals.

"There is a tremendous amount of sensitivity and interest in doing this," says Rosenberg. "If it wants to be successful in the semiconductor space, it needs access to third-party IP in the West. Otherwise, they are not going to fill fabs. Access to third-party IP is crucial in developing world-class consumer-electronics devices."

—by Jeff Berman

▶China Semiconductor Industry Association, www.csia.net/cn.

▶Virtual Socket Interface Alliance, www.vsia.org.

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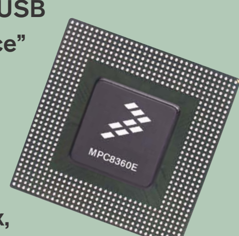

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BY BONNIE BAKER

Big thermal challenges come in small packages

To ensure system reliability, thermal evaluation is a requirement with any size IC. A few simple calculations can help designers estimate and evaluate the thermal behavior of ICs, and lab testing verifies the calculated conclusions.

Consider a dual-LDO (low-dropout) regulator in a DFN8 (eight-pin, dual-flat no-lead) package. Dual LDOs convert one battery input voltage to two lower output voltages with approximately twice the power dissipation of one LDO. In addition, smaller-package DFN8 LDOs have lower thermal resistance than their larger counterparts.

In **Figure 1a**, with an input voltage of 4.2V, regulator 1 (LDO_1) inside the DFN8 package generates an output voltage of 2.8V at 300 mA output current (typical), and regulator 2 (LDO_2) generates an output voltage of 1.8V at 150 mA (typical). The dual-LDO power dissipation is 780 mW. The maximum allowable steady-state junction temperature for the dual LDO is 125°C.

The data-sheet specification for the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the DFN8 package is 41°C/W. The four-layer test method in the JEDEC JESD51-5 and JESD51-7 standards defines the DFN8 thermal resistance. In the JESD51 specifications, some conditions of the test are four-layer boards with a copper thickness of 2 oz on the outer layers and 1 oz on the inner layers.

The model in **Figure 1b** shows the elements for a first-order thermal calculation. In this model, power is the current source, temperature is the voltage, and thermal resistance is a resistor. The definitions of the variables are as follows: I_{SOURCE} is the power in watts, T_J is the chip junction temperature in degrees Celsius, T_C is the device case temperature in degrees Celsius, T_A is the ambient temperature in degrees Celsius, $R_{\theta JC}$ is the thermal resistance from the chip junction to the device case in degrees Celsius per watt, $R_{\theta CS}$ is the thermal resistance from the device case to the copper ground plane (pc board) in degrees Celsius per watt, and $R_{\theta SA}$ is the thermal resistance from the device copper ground plane to ambient (air) in degrees Celsius per watt.

If the dual LDO dissipates 780 mV, the rise in temperature at the junction above ambient of the dual LDO is $T_{J(RISE)}=32°C$, using $R_{\theta JA}$ of 41°C/W. The reliability requirement limits the maximum ambient temperature to (125−32°C), or 93°C.

A feasible two-layer layout for the dual LDO shows different results. For example, consider a board with a 0.0625-in. FR4 substrate and 1-oz copper traces, with the traces residing on the top layer and the copper ground plane on the bottom. Using this pc board, the junction-to-ambient thermal resistance ($R_{\theta JA}$) is 78°C/W.

Measuring thermal response with this type of board proves that the rise in temperature under full-load conditions of the dual LDO increases from 32°C (four-layer with vias) to 59°C. Under these conditions, the maximum ambient temperature is (125°C−59°C), or 66°C. This temperature difference is primarily due to lack of internal layers and vias directly into the copper plane, as the JEDEC standard defines. Thus, although data-sheet specifications are accurate, the physical implementation of the product on the pc board weakens the device's thermal performance. EDN

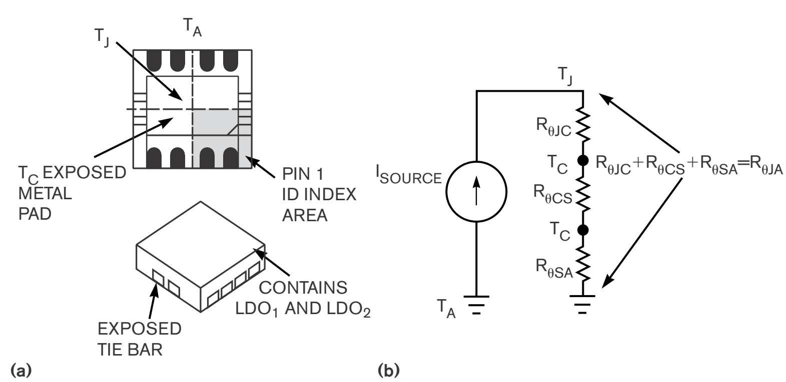

Figure 1 The DFN8 package measures 3×3 mm (a). T_J, T_C, and T_A define the package's thermal model (b).

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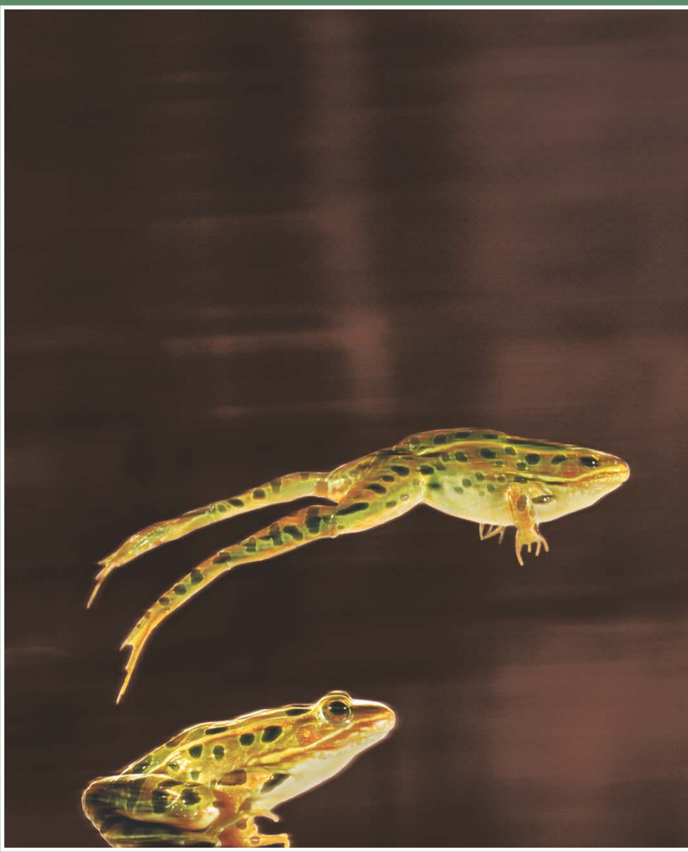

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 BY ROBERT CRAVOTTA • TECHNICAL EDITOR

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Powering to the heavens

How does a liquid-propulsion rocket engine convert liquid mass into enough force for a spacecraft to attain escape velocity?

Rocket engines are reaction engines, in that they throw mass, generally in the form of a high-temperature and high-pressure gas, in one direction to create a reactionary thrust in the opposite direction. The physics of this reaction is simply F=ma, or force equals mass times acceleration. The mass comes from the fuel that the rocket engine burns. The burning process accelerates the mass down through the nozzle of the rocket engine, causing force to push the rocket skyward. The kinetic energy of the combustion products causes the thrust. At this point, the science and art of rocket-engine design come into play.

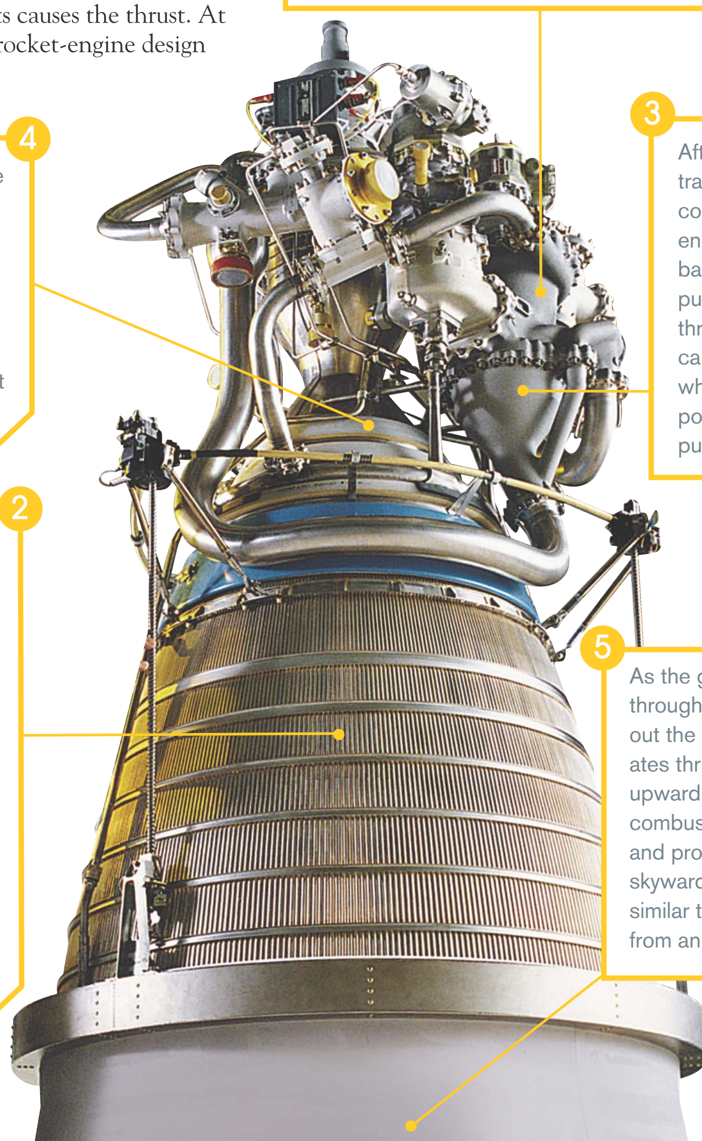
1 Because there is no air in space, liquid-fueled rocket engines need to carry both fuel and oxidizer in external tanks. For some liquid-fueled engines, the fuel is hydrogen or kerosene, and the oxidizer is oxygen. To minimize the required tank volume, extreme cooling liquefies these propellants. The pumps must elevate the pressure of the propellants when they leave the tanks to overcome the pressure that the burning fuel creates in the combustion chamber.

2 After leaving the pumps, the propellants pass through the coolant passages. The coolant passages are necessary because burning propellants within the combustion chamber and nozzle create high temperatures that could melt these areas. Supercooled propellants passing through the coolant passages prevent the combustion chamber and nozzle from melting. The process of cooling the combustion chamber and nozzle also heats the propellants in preparation for entry into the combustion chamber.

3 After the propellants travel through the coolant passages, the engine routes them back into the turbopump. They pass through a turbine, causing it to rotate, which provides the power to turn the pumps.

4 The fuel and oxidizer enter the combustion chamber, where they ignite and burn to form a superheated, high-pressure gas. The pressure that this process creates forces the gas through a narrow passage called the throat and out the nozzle.

5 As the gas accelerates through the throat and out the nozzle, it generates thrust that pushes upward toward the combustion chamber and propels the rocket skyward. This process is similar to air escaping from an inflated balloon.



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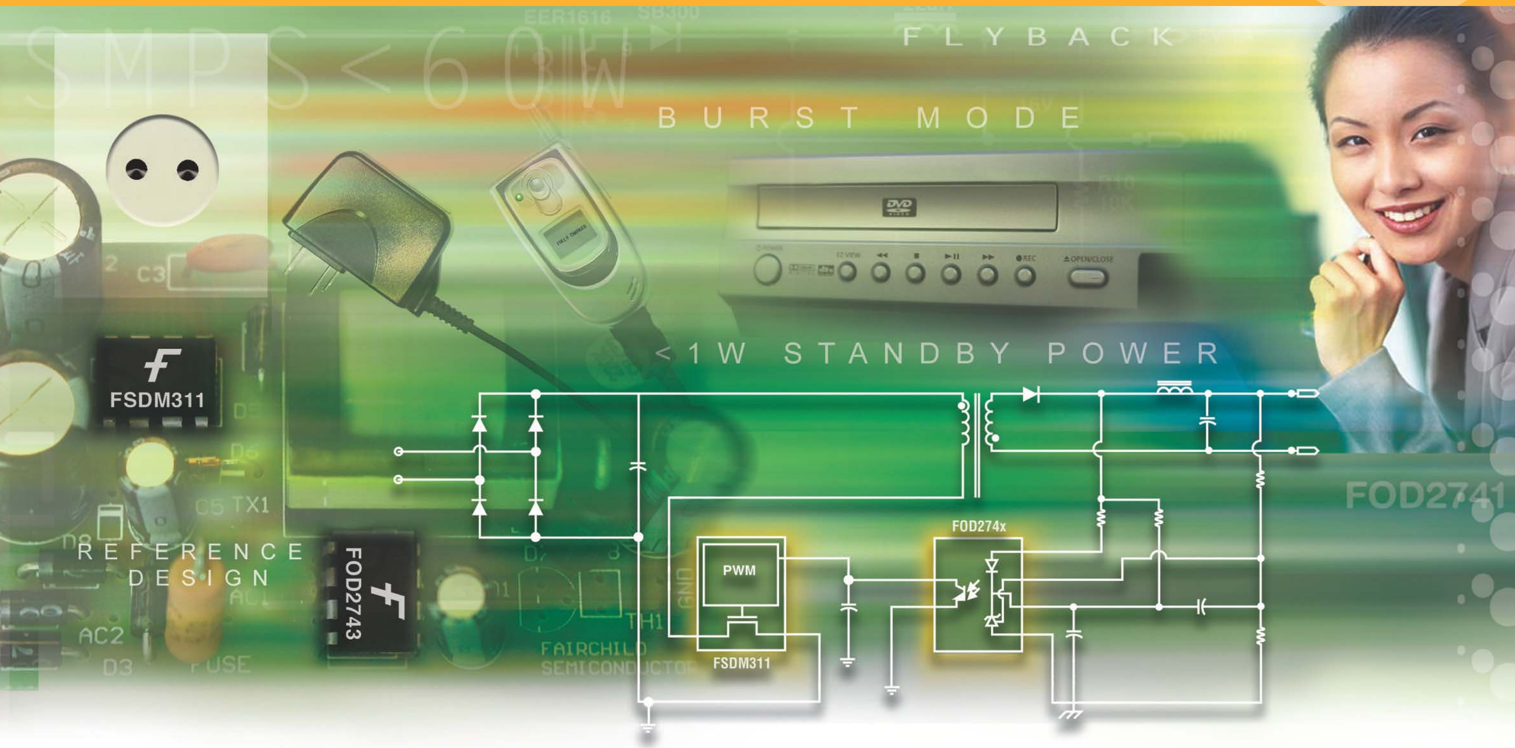

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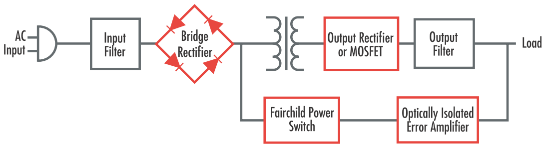

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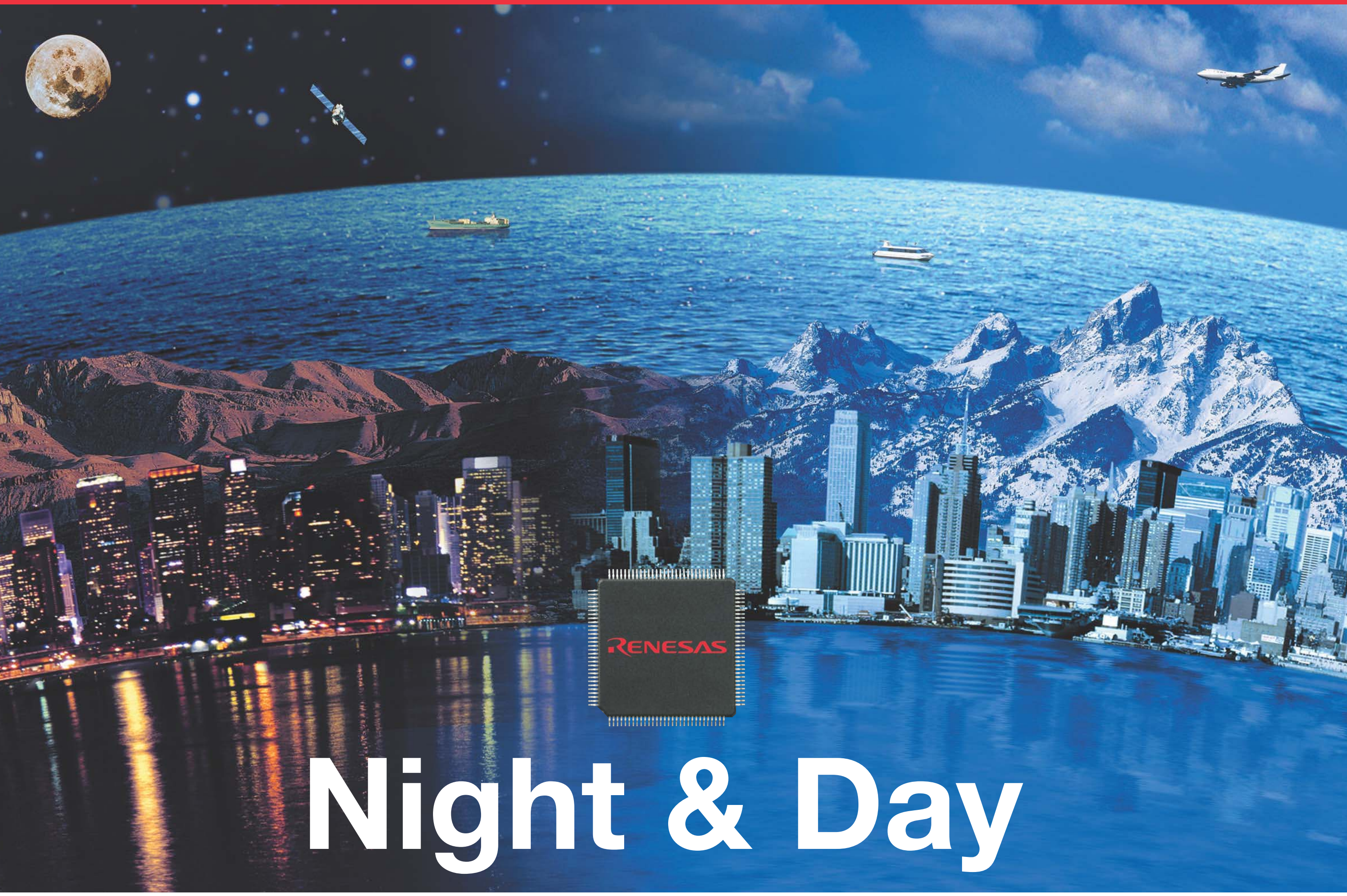

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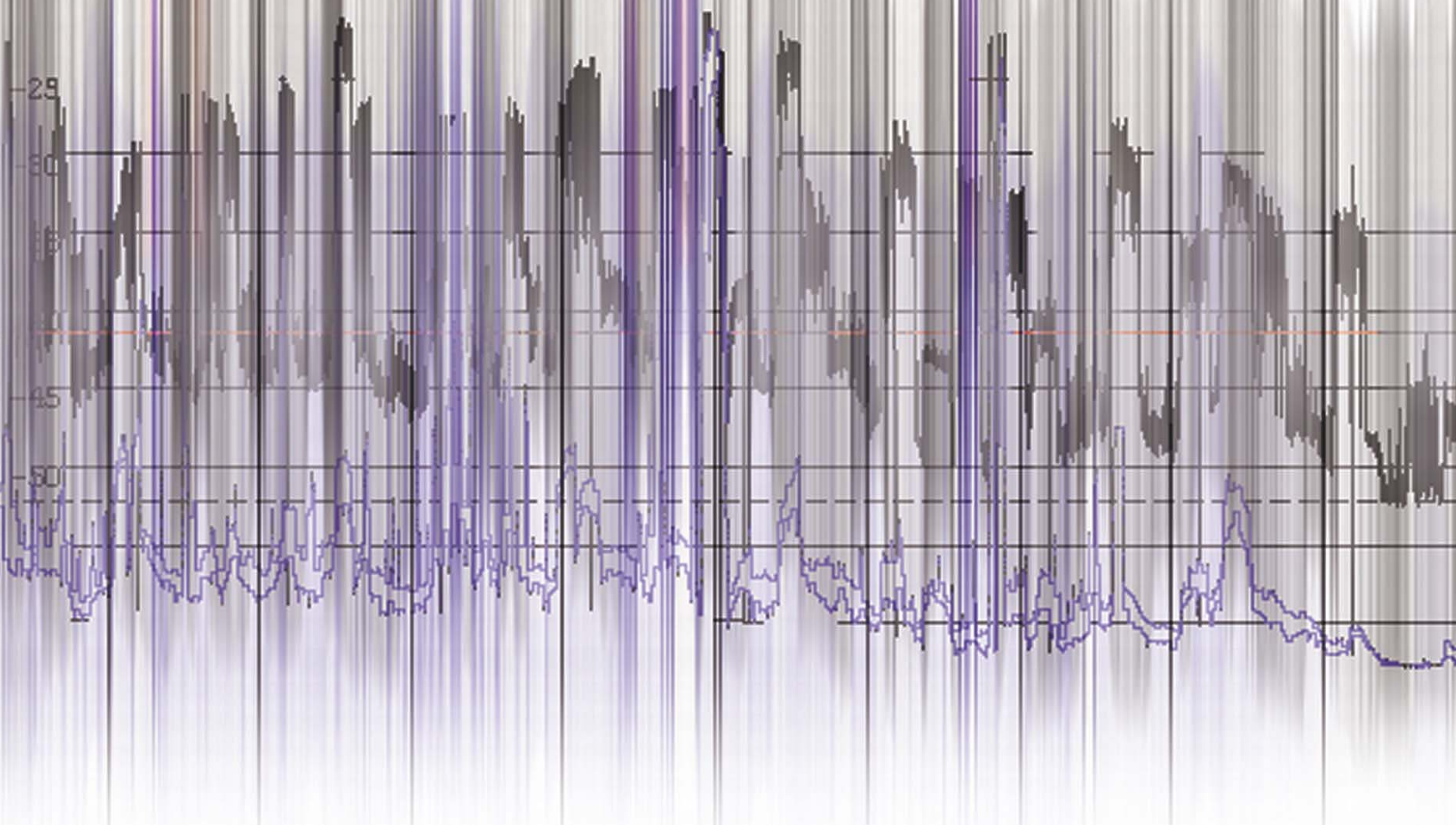

BY DAN STRASSBERG • CONTRIBUTING TECHNICAL EDITOR

Testing UWB: Don't try this at home!

ULTRAWIDEBAND WIRELESS COMMUNICATION MAY BE THE WAVE OF THE FUTURE, BUT ENGINEERS WHO LACK SOLID RF-TEST EXPERTISE WILL NEED ASSISTANCE FROM AN EXPERIENCED TEST LAB TO ESTABLISH UWB-PRODUCT COMPLIANCE WITH FCC SPECS.

If many of the best-known electronics companies—and a large number of smaller start-ups—get their way, UWB (ultrawideband), the new, short-range, ultrahigh-speed wireless-communication technology, will soon transform communication among computers and peripherals and among consumer-electronic devices—at least in the United States. What's more, Japan appears close behind. Meanwhile, Europe seems to be taking a wait-and-see position on UWB.

In the United States, the FCC (Federal Communications Commission) has allocated a 7.5-GHz-wide swath of spectrum—3.1 to 10.6 GHz—to UWB. If you haven't yet read about the technology, your reaction may be, "How can it do that? Other services are already using most of that spectrum." The answer is that UWB, by design, sends signals at such low average power (−41.3 dBm/MHz) and in such short bursts that the signals appear as low-level noise to the receivers for the other services. Those receivers have enough noise immunity to be unperturbed by the UWB transmissions.

Two industry groups support competing and incompatible forms of UWB. The WiMedia Alliance, of which the MBOA (Multiband OFDM Alliance) recently became part, primarily supports MB-OFDM (multiband orthogonal frequency-division multiplexing); the UWB Forum supports DS (direct-sequence)-UWB, which some—but *not* Forum members—call impulse radio. Both groups are rumored to also support—or at least to be considering support of—a low-cost, lower speed, low-power version of impulse radio, whose key application may be a future version of ZigBee, the wireless-sensor standard.

Both groups' Web sites list large numbers of member companies, but, of the two, the WiMedia Alliance includes more merchant IC manufacturers, including the all-important Intel, and a technology that many—albeit, not UWB Forum members—call more ele-

AT A GLANCE

- UWB (ultrawideband) radio, a shared-spectrum wireless technology, has the potential to transmit data at gigabit-per-second rates over distances of tens of meters without interfering with existing services with which it shares the spectrum.
- The IEEE has not yet reached consensus on a UWB standard, so developers of products that use UWB technology must choose between fundamentally incompatible approaches, each of which claims advantages over the other.
- MB-OFDM (multiband orthogonal frequency-division multiplexing) has broader support among IC makers; DS (direct-sequence)-UWB development is further along.
- Testing products that incorporate UWB technology requires great familiarity with multigigahertz RF measurements and the instruments used to make them.

gant and more readily scalable to higher data rates. The Forum says, however, that its DS-UWB technology uses less power to achieve equivalent range—a key attribute in battery-powered-system applications—and is both inherently simpler, thus less costly, and closer to market readiness than is the Alliance's computationally intensive MB-OFDM. The Alliance disagrees on several counts. As Jason Ellis, senior manager of business development and marketing at Alliance member Staccato Communications, puts it, "Real MB-OFDM devices cost substantially less and use less power." However, a Forum spokesman insists that the DS-UWB parts perform more required UWB functions than do the MB-OFDM parts that Alliance members are using for comparison and that if comparable parts of both types existed, the DS-UWB parts would cost less and use less power.

DIFFICULT DECISION

Early adopters of UWB will, therefore, need to choose between the two major approaches, and, in choosing, they will have to decide whether they think the Alliance's lead in industry popularity trumps the Forum's lead in developing its technology. At one time, the UWB Forum had proposed a CSM (common signaling mode), which would allow MB-OFDM and DS-UWB systems to communicate with each other at low data rates. The WiMedia Alliance has declared the CSM idea dead, but Forum members say that CSM can't and won't die unless one of the two technologies disappears, because, without it, neither type of system can detect the presence of nearby systems of the other type. The result, they insist, will be interference that may prevent either type of system from working satisfactorily.

For a wireless technology, UWB can be blazingly fast. According to Alliance members, early MB-OFDM-based products will permit data rates as high as 480 Mbps at a 3m distance and 110 Mbps at 10m. In a few years, these folks say, speeds should reach 1 Gbps at perhaps as much as 20m. Unfortunately, when quoting these performance figures, the Alliance members sidestepped the issue of BER (bit-error rate) or PER (packet-error rate). Without that information, the data rates are not particularly meaningful.

Alliance members assert that the 10^{-12} error rates of which Forum members speak represent overkill in the area of the UWB market that many in the Alliance consider the most lucrative—consumer multimedia applications. Nevertheless, Freescale Semiconductor, the Forum's principal merchant-IC-manufacturer member, was first to announce an agreement to supply UWB devices to a major consumer-electronics manufacturer (Haier). Freescale was also first to deliver fully operational UWB silicon (with a raw data rate of 114 Mbps at 20m) and expects late this

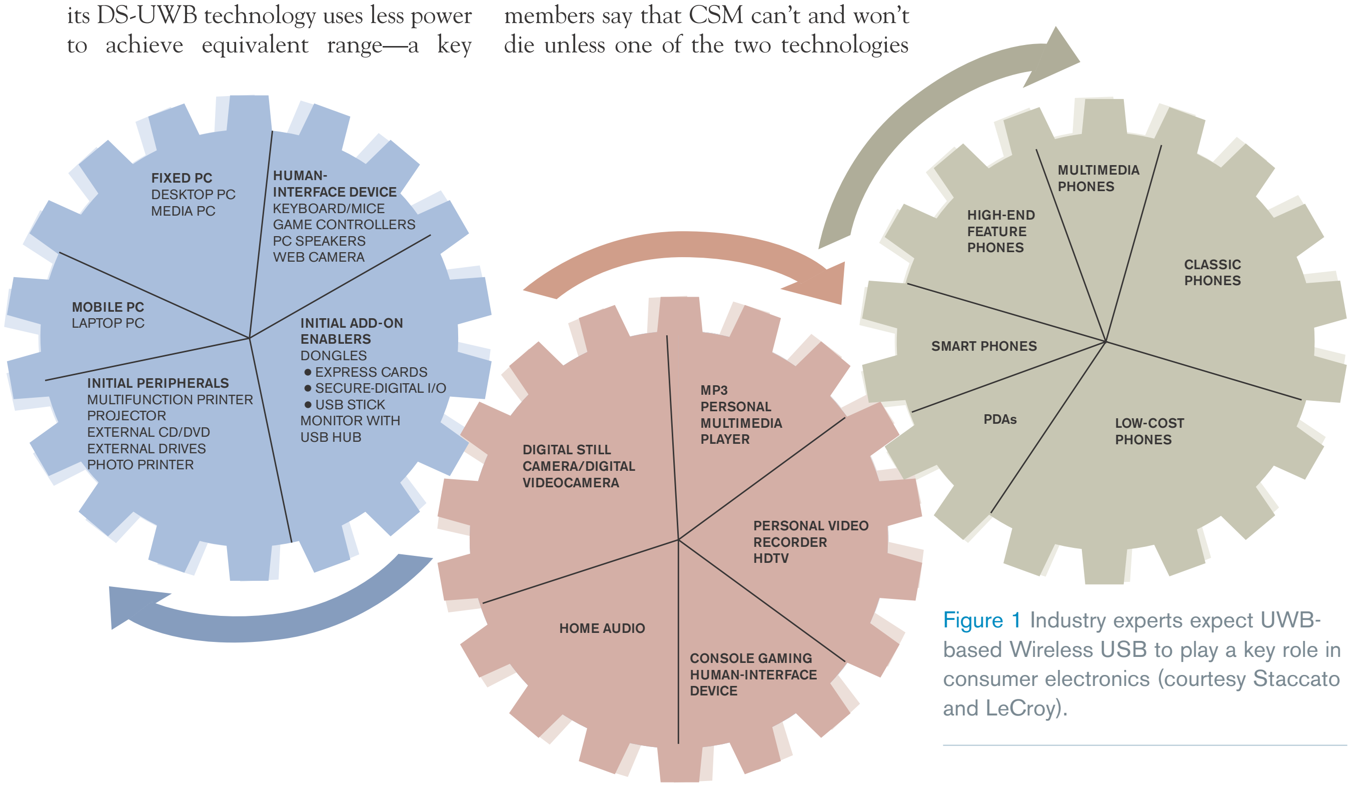

Figure 1 Industry experts expect UWB-based Wireless USB to play a key role in consumer electronics (courtesy Staccato and LeCroy).

year or early next to announce parts almost six times as fast. The company also questions whether 16-QAM (16-level quadrature-amplitude modulation), which the Alliance recently specified for data rates greater than 200 Mbps, can really achieve 10m range and still meet the FCC's −41.3-dBm/MHz radiated-power limit, because, says a Freescale spokesman, "16-QAM takes approximately 4 dB more power per bit to go the same distance as DS-UWB's bipolar- and quadrature phase-shift keying."

How the UWB market divides among several segments will determine the kinds of products chip and module manufacturers emphasize (see **sidebar** "UWB drives to commercialize"). A key UWB application is almost certain to be WUSB, a wireless version of the Universal Serial Bus, whose wired embodiments truly dominate connections between peripheral devices and PCs. Industry watchers seem to agree, however, that growth of USB for peripheral interconnection has slowed and that sales of USB components—ICs, for example—for home-multimedia applications now exceed sales of such components for use in PCs and peripherals. This trend is like-

UWB DRIVES TO COMMERCIALIZE

By Roberto Aiello, Staccato Communications

The stars must be in proper alignment for any new technology to come to market, and, for UWB (ultrawideband) communication, the key items are international standards, market pull, and the availability of commercially viable products. All these elements are lining up, and consumer products will feature high-speed wireless connectivity for the 2006 holiday season.

For wireless communications, regulatory agencies must define the first piece, spectrum allocation, before organizations can establish standards. On Feb 14, 2002, the FCC (Federal Communications Commission) issued a Report and Order allocating 7.5 GHz of unlicensed spectrum for UWB devices operating in the 3.1- to 10.6-GHz frequency band. This move legitimized the technology and fueled the urgency to understand the customer requirements and to have the technology mature within an open-industry-standards forum. Outside the United States, worldwide regulatory agencies are in varying stages of developing regulations and, in most industrialized countries, should soon issue rulings.

The standards activities began within an IEEE committee, and, in an effort to accelerate and streamline standardization, the MultiBand Coalition formed in September 2002. The coalition later became the MultiBand OFDM (orthogonal-frequency-division-multiplexing) Alliance and this year merged with the WiMedia Alliance to become an open industry association for promoting and enabling the rapid adoption, regulation, standardization, and multivendor interoperability of UWB. WiMedia-based UWB specifications target use in wireless personal-area networks that operate at speeds as high as 480 Mbps and provide low-power multimedia capabilities for consumer, mobile, and automotive markets. Emphasizing peaceful coexistence with other wireless services, WiMedia's UWB common platform operates with application stacks that the Wireless-USB Promoter Group, the 1394 Trade Association's Wireless Working Group, and the Bluetooth-SIG developed. IEEE and Ecma-International standards committees are currently reviewing the platform specs.

MARKET PULL

WiMedia UWB technology, which will debut as Certified Wireless USB, is fulfilling a market need by enabling popular, high-performance wired approaches to evolve into wireless approaches. Developers are designing the technology, which extends to support Wireless IEEE 1394, Internet protocol over UWB, and next-generation Bluetooth, into computers, peripherals, home-entertainment equipment, mobile phones, and other consumer-electronic devices. Through UWB, these products will rid themselves of unsightly rats' nests of cabling.

As with any technology en route to market, price is a key concern; multivendor interoperability, form factor, and performance are also important. With the history of Bluetooth and WiFi (Wireless Fidelity) as benchmarks, vendors know that, to achieve mass-market adoption of their products, designers must implement them in all-CMOS semiconductors. Besides low cost, the all-CMOS approach provides outstanding performance in small packages, thanks to high levels of integration.

Staccato Communications and other UWB-semiconductor companies have recently entered the final stage of launching a technology: compliance and interoperability testing. Things are looking good: The developers of Certified Wireless USB built on established compliance programs that have enabled more than 2.5 billion USB connections. We are well on the way to seeing UWB-based products late in 2006.

AUTHOR'S BIOGRAPHY

Roberto Aiello is co-founder and chief technology officer of Staccato Communications. He holds a doctorate in physics from the University of Trieste (Italy) and is the author of more than 20 patents on UWB technology.

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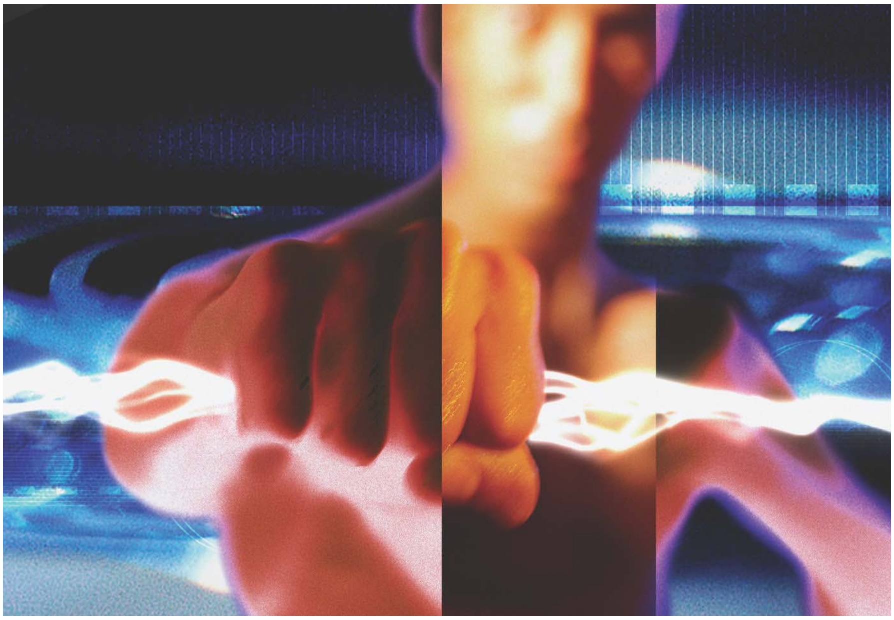

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SP3073E	1Tx/1Rx	full	500kbps	±15kV	14 Pin NSOIC
SP3074E	1Tx/1Rx	full	500kbps	±15kV	8 Pin NSOIC
SP3075E	1Tx/1Rx	half	500kbps	±15kV	8 Pin NSOIC
SP3076E	1Tx/1Rx	full	16Mbps	±15kV	14 Pin NSOIC
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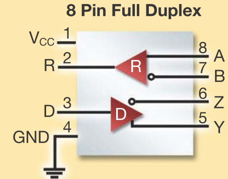

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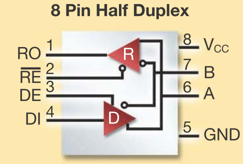

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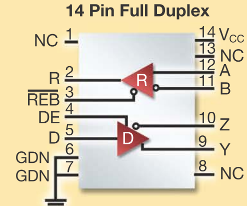

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ly to accelerate in WUSB; although there is little probability of a rush to substitute printers that use WUSB for units having wired connections, observers expect WUSB and a UWB version of IEEE 1394 (FireWire) to rapidly supplant wired connections among components of large-screen high-definition-TV systems (**Figure 1**).

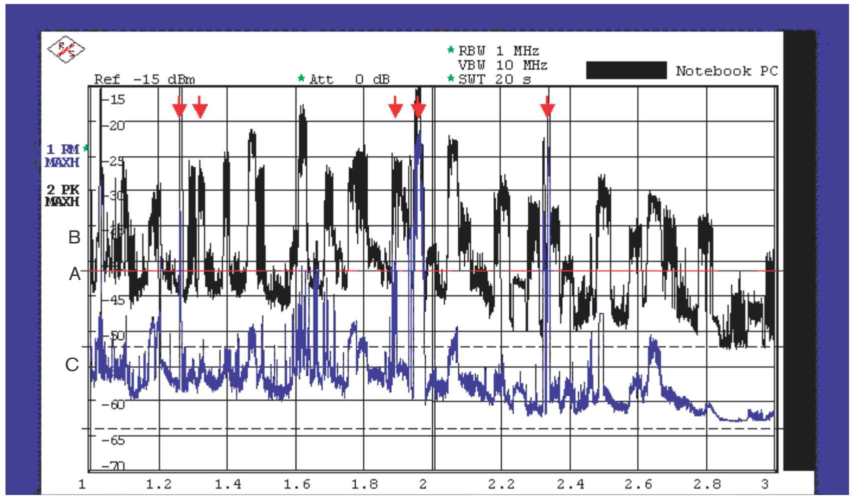
DOUBTERS AND DETRACTORS

UWB, like any other technology that is new and unproven in commercial applications, has doubters and detractors. In this case, many detractors fear that UWB will interfere with the other services whose spectrum it shares. UWB raises barely a whisper of concern, however, compared with another currently trendy shared-spectrum communication technology, BPL (broadband over power lines—see **sidebar** "BPL: the uninvited guest").

In a move to pre-empt problems, UWB-system architects have removed from the range of frequencies that UWB occupies the area in the vicinity of 5 GHz, which is home to several of the newer forms of wireless networks, such as IEEE 802.11a, g, and n, whose narrowband signals might otherwise cause interference to UWB signals. In addition, to avoid interference with the GPS (global positioning system), the FCC not only restricts UWB to frequencies well above those that GPS uses, but also demands stringent testing of UWB products and systems for out-of-band emissions at or near GPS frequencies.

The feeling in the UWB community is that the FCC has gone overboard in restricting the field strength of UWB emissions, even though, in some other technologies, such as BPL, the commission appears to have yielded to political pressures and ignored—or at least downplayed—legitimate concerns about interference to established services.

Currently, however, limits that UWB developers regard as excessively strict on EMI (electromagnetic-interference) emissions from UWB transmissions make compliance measurements more difficult, expensive, and time-consuming than the developers feel they need to be and can sometimes even make meaningful measurements impossible. Moreover, the limits are often far below FCC limits on and actual emissions from portions of the equipment under test that are unre-



NOTES:
RBW=RESOLUTION BANDWIDTH.
VBW=VERTICAL BANDWIDTH.
SWT=SWEEP TIME.

Figure 2 Unintentional emissions from common products that have no UWB capabilities exceed the FCC UWB-emissions limit of −41.3 dBm/MHz (Trace A, red). Even though intentional UWB emissions are limited to 3.1 to 10.6 GHz, the limit also applies to out-of-band emissions, such as those shown, from a popular notebook PC. Trace B (black) shows the peak emissions. Trace C (blue) shows the rms emissions. The blue-trace peaks rise well above the FCC limit–particularly in the GPS bands denoted by the red arrows. The peaks were present even when the PC was off, albeit still connected to ac power (courtesy Freescale).

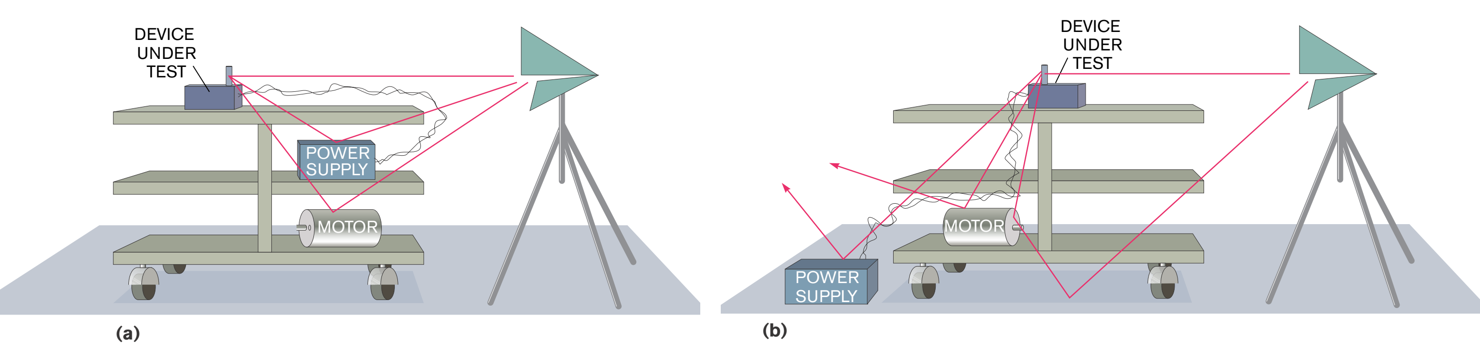
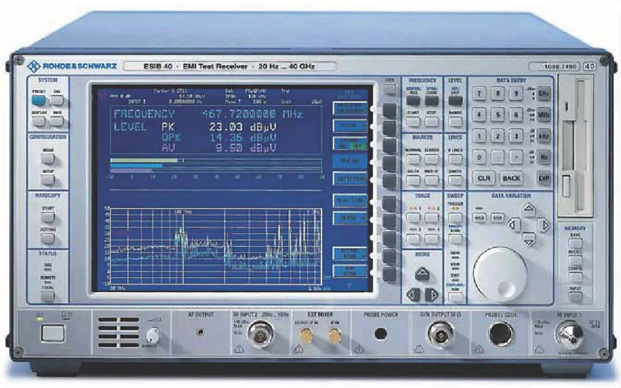


Figure 3 The physical arrangement of test equipment can render UWB-emissions measurements meaningless. Reflections from the device under test, its power supply, and a motor result in unstable readings (a). Rearranging these components solves the problem (b) (courtesy Freescale).

lated to UWB. These emissions—for example, from PC power supplies and processor ICs—are present whether or not UWB is in use and can so completely dwarf those from UWB that, when UWB is activated, its contribution is undetectable (**Figure 2**).



EMI (electromagnetic-interference) test receivers, such as this unit from Rohde and Schwarz, are among several specialized classes of instruments that play major roles in the testing of products that implement UWB.

BIG DIFFERENCES

DS-UWB and MB-OFDM differ profoundly. DS-UWB is sometimes referred to as a zero-carrier system because some implementations do not use conventional modulation of a sinusoidal carrier. The bandwidth can exceed 25% of the signal's center frequency, however. For example, signals that occupy a frequency range of 3.1 to 4.9 GHz have a center frequency of 4 GHz and a bandwidth of 1.8 GHz, which is 45% of the center frequency. In this type of UWB, the signals can be on for a few nanoseconds or, in some cases, even less than 1 nsec and can be off for considerably longer periods.

MB-OFDM is not a zero-carrier system; it uses a large number of carriers. Because attempting to continuously use the full 1.8 GHz would enormously increase the design complexity and might increase the power requirements beyond acceptable limits, the WiMedia Alliance system divides the 3.1- to 4.9-GHz spectrum into three bands, each slightly wider than 500 MHz, and periodically switches the signal among the bands. Each band contains 128 OFDM carriers, each of which is modulated either by QPSK (quadrature-phase-shift keying), which transmits two bits per symbol, or at higher data rates, by 16-QAM, which transmits four bits per symbol. The OFDM carriers are *not* subcarriers, however; there is no main carrier.

The ensemble of modulated carriers occupies one of the 500-MHz-wide bands for 250 nsec. Then, after a short delay, it switches to one of the other two 500-MHz-wide bands for another 250 nsec. Then, after another short delay, it switches to the third 500-MHz-wide band for another 250 nsec. The process repeats approximately every microsecond. A key reason for occupying three 500-MHz-wide bands, each for less than one-third of the time, instead of continuously occupying just one 500-MHz band, is to hold down the average energy radiated in any one band—and, hence, across the entire 1.8 GHz—to comply with the FCC radiation limits. According to the UWB Forum, however, the band-switching approach raises by 6 dB the ratio of peak-to-average signal, preventing operation at the FCC's maximum permitted level, thereby reducing the range.

The reason for using only the lowest one-fourth of the allocated 3.1- to 10.6-GHz spectrum is to stay in a frequency range that is compatible with current, well-understood, cost-effective CMOS-

BPL: THE UNINVITED GUEST

Any technology that moves into the spectrum space that other communication services already occupy is bound to create consternation among users. A case in point is BPL (broadband over power lines). Unlike short-range, wireless UWB (ultrawideband), which users generally consider to be a well-mannered guest, BPL is a medium-range wired technology, whose critics insist that its key shortcoming is an inability to confine its signals to the power lines over which they are supposed to travel. BPL's appeal is its use of ac-power wiring, which is virtually everywhere that people are. Unfortunately, the power wiring is also BPL's potential undoing.

Power lines are meant to convey ac at 50 or 60 Hz–not signals at the higher frequencies that BPL uses. When they travel over power lines that weren't designed to carry them, those frequencies too readily escape into the air, where they can become uninvited interlopers in many forms of wireless communication and can cause myriad problems.

Power-line communication has existed in various forms for three decades or so but has achieved only limited success. Every few years, someone resurrects the idea, promising even higher data rates, at which the technology then fails anew when facing real-world conditions. Often, the problem is unreliable data transmission–a consequence of power lines' uncontrolled high-frequency characteristics, which change continually with variations in the ac load. Although major companies–most recently, Google (www.google.com)–have invested heavily in BPL, cynical critics offer the tongue-in-cheek suggestion that power-line communication should adopt the slogan "the technology of tomorrow–now and forever."

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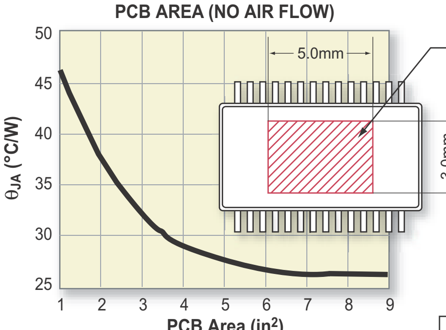
HTSSOP THERMAL RESISTANCE vs PCB AREA (NO AIR FLOW)



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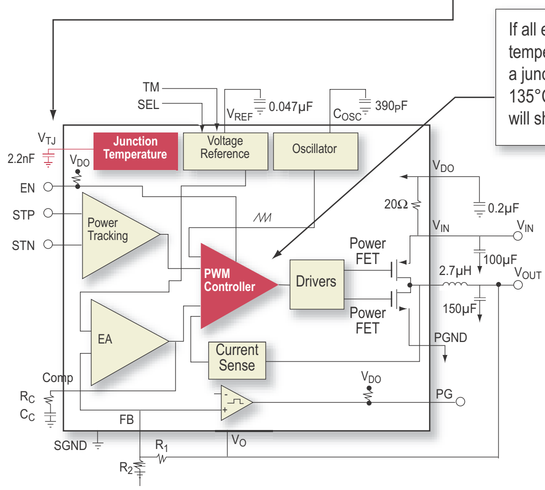

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IC-fabrication technology. As IC manufacturers develop faster processes, the Alliance expects UWB to occupy nearly all of the allotted 7.5-GHz-wide spectrum.

WHAT TO TEST

"In testing a new-product design that incorporates UWB, four major areas require attention: conformance to regulatory requirements, performance, interoperability, and fairness," says Yoram Solomon, mobile-connectivity-solutions director for strategic marketing and industry relations at Texas Instruments (see **sidebar** "Ensuring fair sharing of the UWB channel"). At this stage of UWB's evolution, you must regard all of the areas as challenging. Many of the required measurements are inherently difficult, and developers haven't yet had the opportunity to learn through their own and others' experience most of the lessons they need to learn about what to do and what to avoid (**Figure 3**).

Only those who have access to a properly equipped compliance laboratory and who have significant knowledge and experience in RF measurements and the use of sophisticated RF-measurement instruments should attempt to make the FCC-required compliance measurements. In the absence of those prerequisites, opportunities abound to spend weeks of precious time and huge sums of money on meaningless measurements. Also, because you usually won't find out until much later that the measurements were meaningless, you risk basing costly, yet inappropriate decisions on them.

Mike Violette, chief executive officer of Washington Laboratories Ltd, an FCC-listed test lab in Gaithersburg, MD, makes the following comments: "There are about 170 FCC-listed labs in the United States and half-again as many overseas." You can get the full list from the FCC Directory of Test Labs. "There is no particular designation for labs that are allowed to do UWB testing; any listed lab that has the right equipment and know-how can do it," says Violette.

NOT CHEAP

"One critical aspect of doing the testing is that the necessary equipment isn't cheap," Violette says. "The biggest issue is the available RBW [resolution bandwidth]. One of the UWB tests requires measuring 'power in a 50-MHz band.' To properly do this test, you need a receiver

ENSURING FAIR SHARING OF THE UWB CHANNEL

By Yoram Solomon, Texas Instruments

The WiMedia UWB (ultra-wideband) approach comprises the PHY (physical) and MAC (media-access-control) layers. For applications above those layers, including Wireless USB, Wireless 1394, Wireless Internet protocol, and Bluetooth, the MAC provides access to the air medium through the PHY. Without a fairness policy, the MAC could grant an application access to the radio channel for as long as the application asks. Such unlimited access could, however, cause a serious problem. Several WiMedia links may be active within the same area, and all active links may simultaneously seek access to the radio channel. Because the UWB allocation offers a wide radio spectrum per channel, few channels are available to the links. Without the fairness policy, no device will likely get the desired channel access, and the resulting interference among channels will render all channels useless.

The fairness policy is a set of rules, typically implemented in firmware and running within the MAC. Those rules use the MAC services and ask for fair, effective, and efficient access to the medium. The policy takes into consideration the types of devices seeking access to the medium. Some devices and their links require isochronous access with guaranteed bandwidths and predictable service intervals for streaming multimedia. Other applications may require bulk transfers with low latency. Still others require low power consumption and mobility. The fairness policy's role is to ensure that the applications get the best possible aggregate access to the air channel in accordance with their special requirements.

The policy is also protocol-agnostic. Many protocols, such as those mentioned, can reside on this policy. The fairness policy uses the MAC services through built-in function calls–not according to the type of protocol. The function calls it uses depend on the type of service the application protocol requests and the current usage of the radio channel that the receiver detects. The fairness policy thus optimizes the applications' shared use of the radio channel.

WiMedia developed the MAC as it was developing the fairness policy. When developing this policy, WiMedia's technologists considered the ability to test each of the rules for compliance. Thus, vendors can test every WiMedia-compliant device for fairness-policy compliance. Such testing simulates or emulates an environment with multiple WiMedia devices seeking access to the radio channel while the device under test receives information to transmit. This approach enables testing of the behavior of the device and its adherence to the entire set of rules.

AUTHOR'S BIOGRAPHY

Yoram Solomon is the mobile-connectivity-solutions director for strategic marketing and industry relations at Texas Instruments. He serves on the Bluetooth special-interest group and the WiMedia board of directors and has served as a director of the WiFi Alliance.

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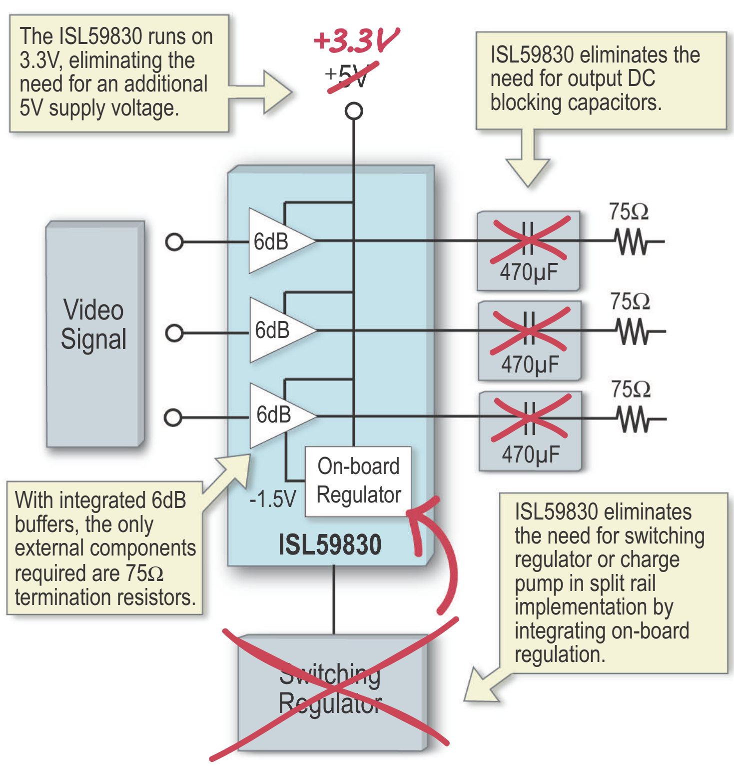
ISL59830 Functional Block Diagram



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or spectrum analyzer with a 50-MHz RBW. To my knowledge, only two units, one from Rhode and Schwarz and one from Agilent, provide both the required resolution and the dynamic range. They are costly and somewhat finicky, too."

John McCorkle, chief technologist of Freescale Semiconductor's UWB Organization, says, "Even with the proper instruments, it is easy to take too few measurements or to allow too little averaging time for rms measurements. To keep from missing narrowband spikes within bands of interest, measurements need to be spaced at 0.4 times RBW-frequency intervals. To obtain accurate rms readings, the detector should dwell at each frequency for 1 msec. If you sweep the frequency instead of changing it in steps, you must set the sweep speed to meet the 1-msec averaging-time requirement. Taken together, the frequency-interval and averaging-time requirements impose a not-insignificant minimum on the time required to perform a UWB emissions test."

Washington Labs' Violette adds, "The other critical aspect of the measurement is that achieving the necessary sensitivity in the GPS bands requires painstaking technique and a very-low-noise measurement path. Also, to get the signal level above the noise, you must place the measurement antenna unusually close to the unit under test. The limits are absolutely too conservative in the GPS bands—something like 30 dB below the general-emissions limits for other FCC-regulated devices, such as computers and other unintentional emitters."

ANOTHER VIEW

At press time, Peter Cain, an expert on UWB testing at Agilent and the author of an application note on the subject (**Reference 1**), commented, "FCC testing isn't the only issue. Regulatory testing is always a subset of the RF testing that a new radio design requires. Regardless of the technology, antenna-based testing always requires attention to detail; the same principles apply to UWB as apply to other [radio] technologies.

"I agree, though, that the levels tested for UWB are low and that you must exercise care to isolate signals not related to the UWB transmitter itself. Building low-noise amplifiers into spectrum analyzers is one way instrument manufacturers can remove the uncertainty of users trying to improvise noise-reduction techniques. Still, how low the emissions have to be depends on more than the other users of the band and the regulatory requirements. Placing the UWB transmitter or receiver near any other radio device or digital device with 'rich' emissions also has an impact. You can, however, desensitize either radio's receiver if the noise floor or out-of-band rejection isn't good enough.

"Before you go to the expense of booking a test at any test house, you should use the wide capabilities of your spectrum analyzer to understand what the device [under test] is doing. The FCC may have chosen certain ways of doing things, but that shouldn't prevent you from working in advance on ways to more quickly identify problems. If you expect your UWB device to be used near any other radio, it is very important to know how the two will interact.

"To overcome long measurement times, you can make the narrow-bandwidth and wide-span measurements with FFT-based techniques instead of swept-frequency ones. Using a 1-kHz RBW automatically guarantees a 1-msec measurement time because the measurement-time window has to be at least several milliseconds. With regard to the 50-MHz RBW requirement, I note that Wisair has just successfully gotten a device through FCC certification without using a 50-MHz RBW filter."

A MATTER OF PROTOCOL

James Wright, director of marketing at LeCroy's Protocol Solutions Group (formerly, CATC), says, "Protocol testing is [yet another] nontrivial area of UWB testing. WUSB will offer more variations and more operating modes than its wired counterparts and will require highly sophisticated protocol-test instruments." LeCroy's initial protocol-test offerings focus on Certified WUSB, a version of WUSB specified by the USB-IF (USB Implementers' Forum). Though the UWB Forum proposed a DS-UWB-based version of WUSB, the USB-IF based Certified WUSB V1.0 on MB-OFDM. Although this development didn't please the UWB Forum, the group still believes that DS-UWB will play an important role in WUSB's future.

Another piece of the UWB-testing puzzle is interoperability testing. The quickest way for developers of UWB products to determine whether their products exhibit interoperability problems is through "unplugfests"—the wireless equivalents of the "plugfests" that organizations responsible for wired protocols have used to great advantage. The events, which have good credibility with special-interest groups and manufacturers alike, bring together for hands-on trials developers of products that are supposed to communicate and work harmoniously with each other. When they detect problems, the developers try to find solutions, and it is not uncommon for competitors to assist one another. Although the WiMedia Alliance hasn't yet announced any unplugfest plans, some members expect that early in 2006 and maybe even sooner, the organization will hold its first such event. It almost certainly won't be the last. EDN

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In his editorial, "Branding the invisible," *EDN Europe* Editor Graham Prophet also takes a look at UWB. Read what Graham has to say at www.edn.com/article/CA484535.

REFERENCE

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AUTHOR'S BIOGRAPHY

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PROGRAMMABLE AUDIO: PART ONE

BY JOSHUA ISRAELSOHN • TECHNICAL EDITOR

A TREND IN SIGNAL-PROCESSING ICs OFFERS SIMPLE AND DIRECT PARAMETRIC CONTROL AND FUNCTIONAL PROGRAMMABILITY. TAKING FULL ADVANTAGE OF FLEXIBLE CHIPS, HOWEVER, MAY DEMAND FLEXIBILITY IN YOUR DESIGN METHODS, AS WELL.

FLEXIBLE SILICON

GUI-programmable audio processors

A simple categorization assigns most signal-processing blocks to one of two groups. On the one hand are generic functions, such as op amps and ADCs, which perform one task and may serve in many disparate applications. On the other hand are application-specific blocks, such as GSM transceivers and 802.11 basebands, that have narrow definitions at a much higher level of functional abstraction and, therefore, perform a more complex set of tasks for only one application. An interesting and growing number of signal-processing blocks lie somewhere in the middle. Further scrutiny reveals that the two categories actually lie on a continuum characterized by a dominantly bimodal distribution with a small but decidedly nonzero population between the groups.

The way designers interact with instances from the two large groups is likewise distinct. Tables of parametric performance characterize single-function generic parts under operating conditions that their manufacturers specify. Part of the design task, then, includes deriving expected circuit-level behaviors from topological analysis and components' spec-table performance. On the other end of the spectrum, conformance to industry standards defines many application-specific blocks. Individual parametric measures may be difficult to extract and impossible to control beyond simply choosing one part over another. In the sparsely populated middle, however, lie parts not given to such easy description. These flexible bits of silicon can take on behavioral attributes that depend on an OEM designer's programming or configuration decisions. But, unlike general-purpose programmable devices, these devices operate at a higher level of abstraction than bytes and words, instantaneous voltages, or individual samples. Instead, these devices operate at a level in which the signal is itself parametric, defined by concepts such as, for example, spectral shape or dynamic behavior. In other words, the functions that these parts offer are not fully defined until you decide what you want them to be, and, unlike with general-purpose signal processors, with these devices, you express those decisions in application-relevant parametric terms.

It comes as no surprise that such devices depend on support hardware and software for evaluation, configuration, and programming. In this first BenchPress project, *EDN* examines the support environments for two devices that exemplify this growing class of signal processor: D2Audio's four-channel, Class D XS-125-4 power-amplifier module and Analog Devices' multichannel, 28-bit AD-1940 audio processor. In this study, both devices process audio signals in ways that readily demonstrate these rather abstract concepts and observations. More important, their evaluation or design-support environments reveal that one's design methods may need to vary to accommodate the nature of these components: Though they may arrive with traditional-looking spec sheets, those familiar documents simply don't—and probably can't—tell the whole story. Flexibility has its costs, and one of them is specificity.

THE BIRTH OF THE BENCH

To get a sense of how these devices and their support environments work in a design setting, I observed two evaluation systems on the bench. The core of *EDN*'s benchtop-test capability for this project is an Audio Precision computer-controlled, dual-domain SYS-2722 audio analyzer—

AT A GLANCE

- The ratings:
  - Flexible silicon parts–great!
  - Support hardware and soft ware–mostly terrific.
  - Documentation–not ready for prime time.
- Software interfaces are convincing, if occasionally cumbersome.
- Though the software tools are mostly quite accurate, be sure to confirm with stimulus/response measurements to prevent unwanted surprises.

itself the teacher of many good lessons (**Figure 1**). Audio Precision equipped the analyzer with an optional lowpass filter that conforms to the AES-17-1998 specification (**references 1** and **2**). The AES-17 filter provides a sharp roll-off for THD+N (total harmonic distortion plus noise) measurements of signal chains that include DACs, signals from which may include a high-level of out-of-band—and thus most often inconsequential—noise (**Figure 2**). The filter removes this ultrasonic noise that could otherwise interfere with the measurement instrument by overloading gain stages or by tripping autoranging thresholds. We wanted to look at a Class D amplifier, so Audio Precision also provided an AUX-0025 switching-amplifier-measurement filter, which prevents the fast edges present on a Class D output stage from inducing slew-rate limiting in the analyzer's input stages.

Additional bench equipment includes a Wavetek-provided handheld Meterman 24XT DMM (digital multimeter) and a Cove Arts-provided HP-3456 bench DMM, HP-6234A power supply, pair of Tannoy Proto-J monitors, and Technics SL-PG480A CD player. The monitors and CD player provided for signal-path debugging and accompaniment.

The Analog Devices AD1940 evaluation board comes complete with a wall-wart power supply and a USB cable, so with the addition only of common signal-interconnect cables, it's ready to go, right out of the box. Power-amplifier tests, however, require appropriate loads, and, in the case of the D2Audio XS-125-4, the necessary load capacity is sizable: The amplifier can deliver 125W per channel into 8Ω. Commercially available loads that large are hard to come by but simple enough to build (see **sidebar** "Light up the iron").

THE ORIGIN OF THE SPECIES

Evaluation boards appear in a number of contexts. IC-design and -product engineers use them to evaluate first-packaged-silicon prototypes. Field-applications engineers use them to help OEM design engineers with part-specific design challenges. Sales engineers use them to demonstrate an IC's capabilities. OEM designers use them as quasiformal development environments. The further along this list you go, the less the operator is intimately familiar with the IC's architecture, modes of operation, programming, strengths, and limitations.

To be sure, the earliest versions of an evaluation board and its software are less polished than those that find their way to customers' hands. The evolutionary track these support tools experience is often divorced from the rigorous product-development methods that the IC enjoys. The evaluation tool's documentation is one area in which this distinction is evident. Though the sophistication of the evaluation tools tends to mimic that of the IC, the sophistication of the documentation tends to follow a different trend—perhaps a trailing indicator of the tool's distribution.

At minimum, any evaluation board should include a map that identifies the location of test points, jumpers, connectors, switches, headers, status LEDs, and any other element of signal, data, power, or human interface. The map, though necessary, is insufficient. The documentation should include a narrative that explains each interface element: settings for switches and jumpers, amplitudes and signaling conventions for test points and connectors, pinouts for headers, and the significance of status indicators—lit, unlit, or flashing. Insufficient documentation results in customer calls to the applications engineer—costly for both the vendor and the customer. This project serves as a case in point: Despite the quality of the evaluation systems, both required application-support calls for questions that the manufacturers could have anticipated and answered in the documentation. Software documentation is no less important. As familiar as GUIs are to anyone in this industry, device- or application-specific elements vary from vendor to vendor and even from product line to product line within a vendor. Functions and attributes that are intuitively obvious to members of an IC-development team may be significantly less so to their customers.

These observations do not in any way mean to beat up on either Analog Devices or D2Audio; they are in good company: It is rare in my experience for any evaluation tool to arrive with the kind of documentation you would expect if the tool were a full-fledged member of the supplier's product line. Good documentation is costly and time-consuming to prepare and maintain. Note, however, that the flip side to the documentation issue is also true: Superior documentation accompanying sophisticated hardware and software helps engineers quickly work their way up a learning curve and reduces the risk to their schedules. They can confirm their understanding of how the IC and its development environment operate. They can spend less time trying to solve

Figure 1 The Audio Precision SYS-2722 dual-domain audio analyzer drives and receives signals on balanced and unbalanced feeds in the analog domain and through balanced, unbalanced, and optical connections in the digital domain.

unanticipated problems and conceptual disconnects and more time driving their projects to successful conclusions.

GETTING CONNECTED

Insufficiently documented or not, these signal processors are bound to provide a memorable first experience. My first exposure to a D2Audio Class D amplifier module occurred in 2003 when system architect and D2Audio cofounder Skip Taylor, PhD, brought a prototype unit for *EDN* to audition. That first amplifier turned in an impressive sonic performance (**Reference 3**), and several subsequent auditions with various production models have since reinforced the initial impression. I had not appreciated the sophistication of the module's signal-processing capabilities until I had a chance to spend some time with the amplifier on the bench; Canvas, D2Audio's GUI-based programming environment, reveals those capabilities.

A D2Audio Class D amplifier module offers programmable signal-processing blocks in a fixed module-specific topolo-

LIGHT UP THE IRON

Despite the fact that audio power amplifiers drive complex impedances, their manufacturers often specify their performance under a resistive load. One reason is that the reactive components of speakers' impedances vary from model to model. Additionally, for any given model, the impedance varies across the audio spectrum. No standard impedance exists. Though manufacturers may test power amplifiers with various speaker-simulation impedance models, the amplifier's data sheet must reflect testing under readily replicated conditions, and, for those purposes, the resistive load is generally preferable.

There's hardly anything conceptually simpler than a resistive load. But to observe D2Audio's XS-125 under various conditions, I wanted a switchable load that could present 4, 8, or 16Ω to the amplifier. Also, because use of a breakaway is always a good idea when working with devices that can deliver substantial energy, I wanted the load switch to be able to disconnect the load resistors from the amplifier if necessary and to do so faster than I could yank banana plugs out of their respective jacks. I'm unaware of an inexpensive, readily available, commercial load with these characteristics; if you know of one, let me know. So, it soon came time to light up the soldering iron and build one (Figure A).

Due to the switching arrangement needed, I switched the load elements with relays. The resistors are all Dale RH-50 8Ω, 50W devices arranged in quads. Because each quad comprises a series set of parallel pairs, the quad's resistance is also 8Ω, but it can dissipate as much as 200W, which gives a moderate margin over the amplifier's 125W/channel capacity.

Relay contacts in the figure appear in their de-energized states corresponding to S_1 up and S_2 in its center-off position. Raising S_2 energizes K_1 and K_3, which connects a pair of quads in series, providing a 16Ω load that can dissipate 400W. Dropping S_2 to its lowest position de-energizes K_1 and K_3 and energizes K_2 and K_4, which folds the resistor string to form a parallel pair of quads. This arrangement results in a 4Ω load that also can dissipate 400W. S_2 is a an Alcoswitch MTL-106E locking toggle switch that requires an operator to pull the toggle bat before it will move to a new position. This requirement prevents an accidental change in the load resistance that the amplifier encounters.

Moving S_2 to its lower position energizes all four relays, which disconnects the load resistors from the amplifier. Normally, I'd design this type of circuit so that all relays in their de-energized state would disconnect the load from its source. In this case, however, I had limited time for procuring parts and equipment, and I wanted to be sure that I had a working 8Ω load even if the power supply, which I used to produce the relay-coil voltage, arrived late.

The availability of the 8Ω, 50W Dale resistors from on-shelf inventory constrained my choice of a parts distributor. The choice and on-shelf inventory of the distributor, in turn, further constrained my choice of a relay. Small, inexpensive PC-mount relays that can switch the load's maximum 10A are not common, so I chose a 12V, DPDT Potter & Brumfield RFE-24012F relay with 8A contacts, and I wired the two poles of each relay in parallel. This gave an acceptable 37% margin.

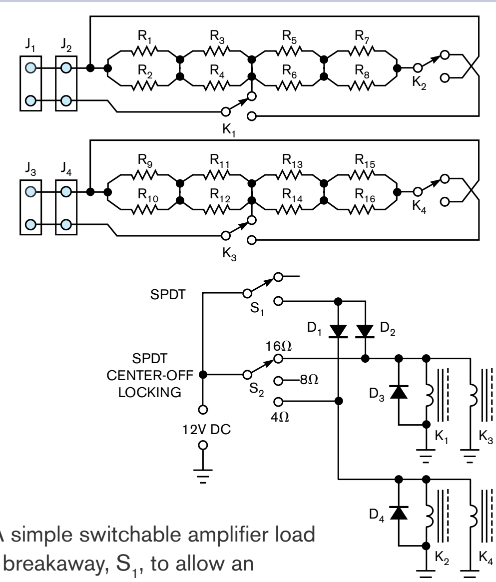

Figure A A simple switchable amplifier load includes a breakaway, S_1, to allow an operator to rapidly disconnect the amplifier. Load resistances correspond to the S_2 toggle position in sequence: 16, 8, and 4Ω.

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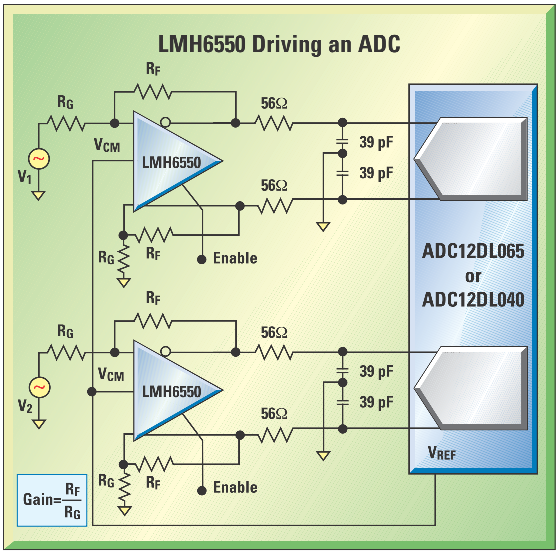

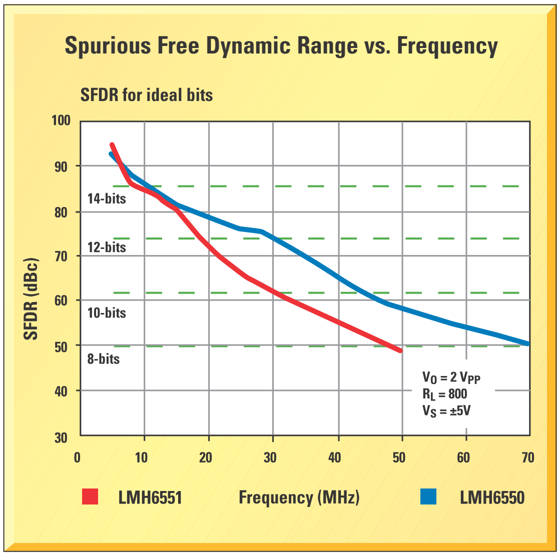

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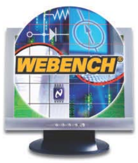

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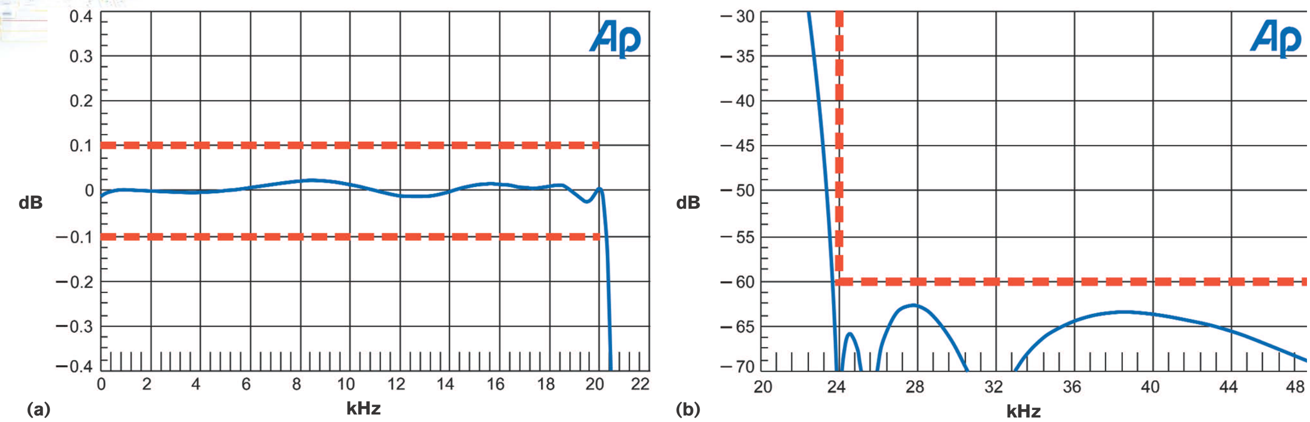

Figure 2 Audio Precision's optional AES-17 filter provides a flat passband with low ripple (a) and better than the −60-dB spec-required stopband attenuation (b) without adding more than 4-ppm THD in the 20-kHz passband. The red lines correspond to the AES-17-1998 spec limits.

gy. The overall structure provides input switching and spectral shaping; a mixer/crossover channel-allocation section; output spectral shaping, delay compensation, low-volume compensation, and dynamic management; channel trims; and a master volume control. Canvas depicts the signal chain in block-diagram form with clickable blocks. Clicking a block launches its associated control panel, and, if the block's function includes spectral shaping, an interactive graph displays a simulated plot corresponding to the current settings (**Figure 3**).

The mixer/crossover block to a great extent defines the overall function of the amplifier. When you configure it as a 4×4 continuously variable crosspoint matrix mixer, you can route any input channel to any combination of output channels. When you set it as a two-output crossover, the block provides a four-to-two channel selector followed by a two-way active crossover network, appropriate for bi-amplified-speaker drives. A three-output-crossover mode allows you to select the signal channel—one of four—and provides triamplified-speaker drives. It also mixes the four input channels through independent level controls and delivers a subwoofer output through a tunable lowpass filter. A four-output-crossover mode uses all of the XS125-4's outputs as a quadamplified-speaker drive. The crossover configurations allow you to choose among Bessel, Butterworth, and Linkwitz-Riley filter sections (**Reference 4**). You can also select Bessel and Butterworth roll-offs of 6, 12, 18, or 24 dB/octave or Linkwitz-Riley roll-offs of 12 or 24 dB/octave.

With signal manipulators on either side of the mixer/crossover block, the XS125-4 architecture appears at first glance to contain design redundancies in both level and spectral controls. Several strategies make different uses of the resources, however, and the appearance of redundancy quickly gives way to an appreciation for having the right controls in the right place along the signal chain. You can invoke the first sets of controls, for example, to correct for deficiencies in the source device or program material and to compensate for room resonances. Two-band tunable tone controls—lowpass and highpass, first-order shelving sections—provide 14 dB of boost or cut. Five-band parametric equalizers provide as much as 6 dB of boost, 30 dB of cut, and Qs of 0.5 to 1442.7. The five bands are identical—each tunable over a 20-Hz to 30-kHz range. The graph that simulates the equalizer's spectral response indicates the interactions of multiple sections. A comparison between the settings and the measured response indicates impressive

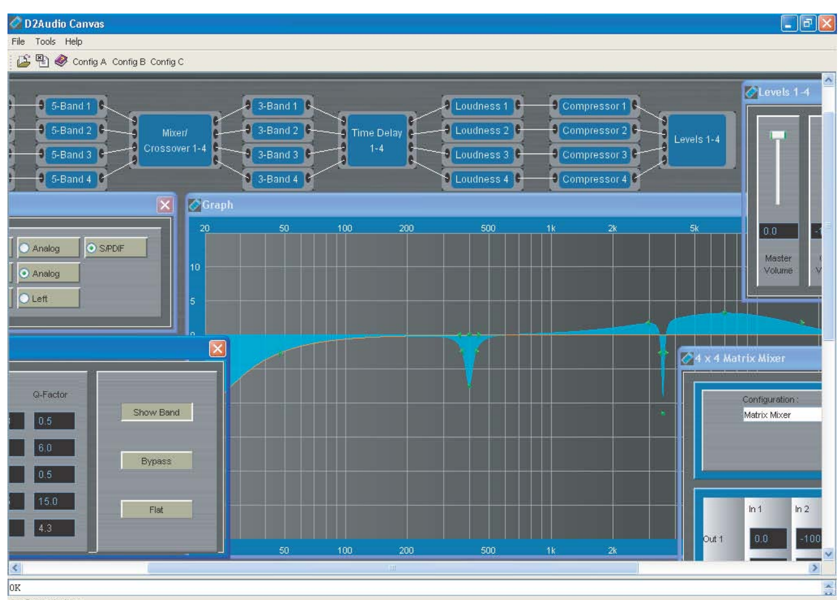

Figure 3 D2Audio's Canvas GUI software provides interactive plots that correspond to spectral-control blocks' settings. Grasping a control point on the plot allows you to rapidly initialize a filter's settings, which you can then fine-tune within the block's control panel.

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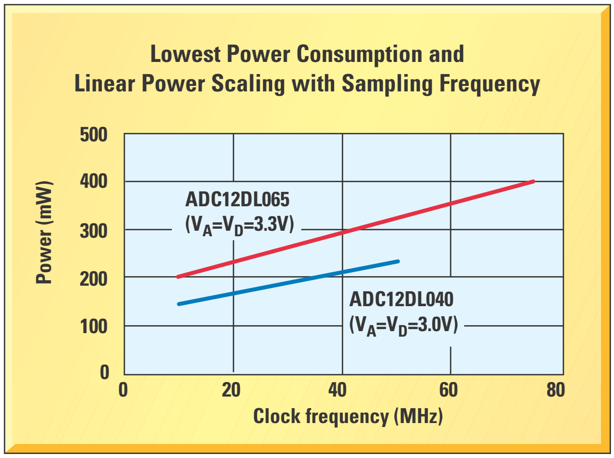

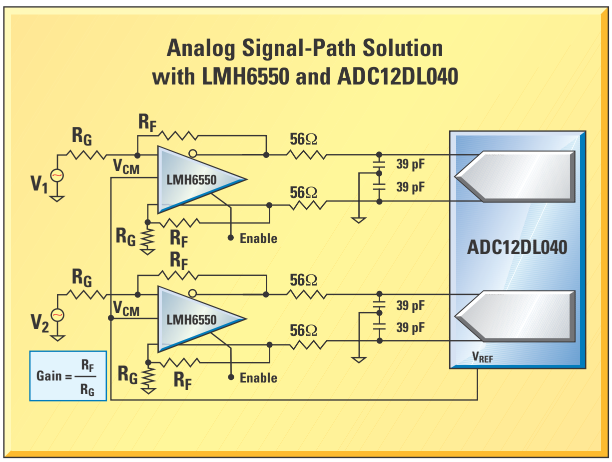

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accuracy in center frequency, cut depth, and Q (**Figure 4**).

You can apply the controls that follow the mixer/crossover block to compensate for output-device-specific deficiencies, such as driver or cabinet resonances, or placement nonidealities. These controls include three-band parametric equalizers with ranges similar to the five-band blocks, 0- to 3.98-msec delays, dynamics compressors, and level trims. The module rounds delay settings to the nearest multiple of the signal-sampling period. A traditional loudness circuit compensates for changes in human spectral sensitivity that listeners experience at low output levels.

You can manipulate tone-control, equalizer, and crossover sections in real time by adjusting sliders within a control panel, typing values into parameter windows within the control panel, or moving control points on the graph. Equalizers feature band-select and section-bypass switches that allow you to make A-B comparisons between a given setting and the system's flat response.

The evaluation hardware platform communicates with a host PC running the Canvas software through a USB connection. During the software launch, Canvas automatically recognizes the module to which it is connected and presents the block diagram appropriate to that module's architecture. Canvas also operates in a simulation mode without a connection to a module. This feature allows you to develop a module configuration offline. It also allows you to familiarize yourself with the features and capabilities of module types other than those you are already using. If a module connects through the USB link, bench experiments indicate that the software ignores attempts to load files created for other module types.

As well-designed as Canvas is, a number of improvements would enhance the software as a development and operating platform. The most obvious of these improvements derives from the fact that multichannel-audio applications virtually always benefit from the concept of channel pairs. Whether the installation implements simple 2.0 stereo or 7.1 surround sound, the option to manipulate channels in pairs is often an asset. One transparent way of implementing channel pairs would allow you to associate blocks within one channel with like blocks in another channel, so that they track each other through a bilateral control link. This sort of parametric tracking is common in digital-audio consoles to ensure, for example, that equalization settings for stereo pairs always stay synchronized across the pair or to allow precise trimming of a channel pair's gain without disrupting the balance. Such systems also allow for fixed delta settings to accommodate minor mismatches between paired channels. Similar tracking is desirable for channel-level trims and crossover settings. In lieu of a tracking function, a quick method of copying and pasting the parameter set as a group from one block to another—or, in the case of multichannel blocks such as the mixer/crossover, from one channel to another—would be welcome.

Dynamic-management blocks require a somewhat more sophisticated type of tracking, and, if D2Audio has implemented this feature in its amplifier modules, it isn't evident from either the documentation or the GUI. When a compressor or limiter acts on one channel of a stereo pair, it must communicate the action it takes to the dynamic-manage-

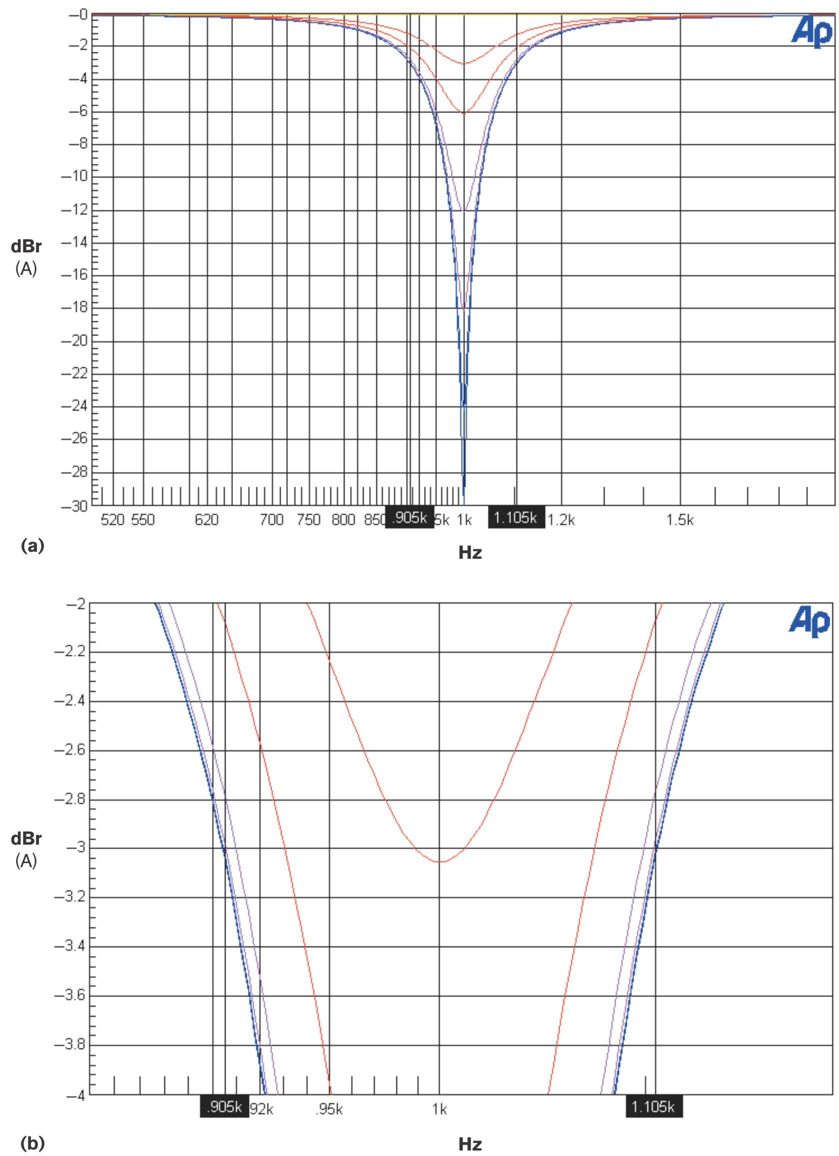

Figure 4 Measurements of the D2Audio XS-125-4's equalizer confirm its performance relative to software settings (a) at 1 kHz with 3, 6, 12, 18, 24, and 30 dB of cut with a Q of 5. A close-up view of the same data reveals the accuracy of the filter's implementation (b).

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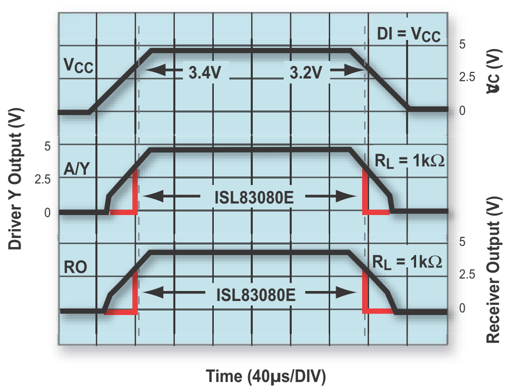

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ISL83082E	1 / 1	256	Half	Yes	Yes	0.115	Yes	Yes	560 / 530	0.07	4.5 to 5.5	8 Ld MSOP 8 Ld SOIC
ISL83083E	1 / 1	256	Full	Yes	Yes	0.5	Yes	Yes	530 / 530	0.07	4.5 to 5.5	14 Ld SOIC
ISL83085E	1 / 1	256	Half	Yes	Yes	0.5	Yes	Yes	560 / 530	0.07	4.5 to 5.5	8 Ld MSOP 8 Ld SOIC
ISL83086E	1 / 1	256	Full	Yes	No	10	No	Yes	530 / 530	0.07	4.5 to 5.5	14 Ld SOIC
ISL83088E	1 / 1	256	Half	Yes	No	10	No	Yes	560 / 530	0.07	4.5 to 5.5	8 Ld MSOP 8 Ld SOIC

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ment block attached to the other paired channel. Both analog and digital compressors implement this function by means of a stereo-link, or side-chain, port. Lacking this link, a sound source that appears predominantly on one side of the stereo image and that exceeds the compressor's threshold, causes that channel's compressor to reduce the channel gain but leaves the opposite channel unaffected. The result is that the entire stereo image shifts toward the opposite channel until the triggering event has passed, and then it shifts back again. A stereo link and identical compression settings cause identical gain reduction in both channels even if the program material exceeds the threshold on only one of the channels. This behavior maintains the stereo image as it was originally constructed and allows less obtrusive dynamic control.

The choice of crossover-filter type is complex and may well include subtleties unfamiliar to many OEM designers. The Linkwitz-Riley crossover, though increasingly popular, is less broadly understood than Bessel and Butterworth characteristics, which were well-established in the literature long before then-Hewlett-Packard engineers Siegfried Linkwitz and Russ Riley revealed their approach in 1976. In any event, the fact that D2Audio provides the choice of three filter types suggests that the company understands the value of all three. Either a section within the Canvas documentation or a separate white paper explaining D2Audio's view on this topic would help guide OEM designers who use the crossover block.

Despite these few criticisms and suggestions, the Canvas software environment, the D2Audio evaluation hardware platform, and the amplifier modules work together seamlessly and present a shallow learning curve to OEM designers incorporating these amplifiers in their systems.

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Joshua Israelsohn
at jisraelsohn@edn.com.

In Part Two, the Analog Devices AD1940 evaluation board and SigmaStudio GUI software have a turn on the bench. Look for it in the Oct 27, 2005, issue of *EDN*. EDN

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2. "S-AES-17 Low Pass Filter," Audio Precision, www.audioprecision.com/index.php?page=products&id=1000000203.
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Using Resistive Touch Screens for Human/Machine Interface

By Rick Downs • *Applications Engineering Manager, Data Acquisition Products*

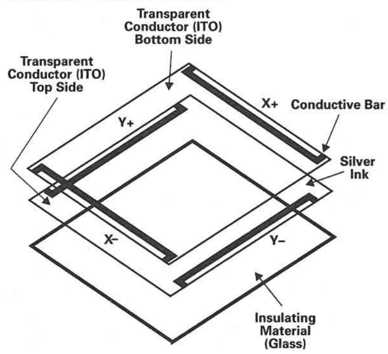
Introduction

Touch-screen interfaces are effective in many information appliances, in personal digital assistants (PDAs), and as generic pointing devices for instrumentation and control applications. Getting the information from a touch screen into a microprocessor can be challenging. This article introduces the basics of how resistive touch screens work and how to best convert these analog inputs into usable digital data. Issues such as settling time, noise filtering, and speed trade-offs are addressed.

Resistive touch screens

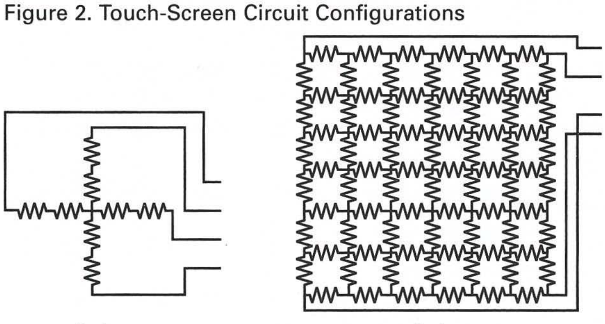
Resistive touch screens consist of a glass or acrylic panel that is coated with electrically conductive and resistive layers made with indium tin oxide (ITO) (see Figure 1).

Figure 1. Resistive Touch Screen



The thin layers are separated by invisible spacers. Resistive screens are generally the most affordable type of touch screen, which explains their success in high-use applications like PDAs and Internet appliances. Although clarity is not as good as with other touch-screen types, resistive screens are very durable. The only concern is that the resistive layers can be damaged by a very sharp object. The two most popular resistive architectures use 4-wire or 5-wire configurations, as shown in Figure 2 (the 5-wire configuration uses the second layer as a wiper contact, not shown here). The circuits determine location in two coordinate-pair dimensions, although a third dimension can be added for measuring pressure in 4-wire configurations. Texas Instruments (TI) offers specialized analog-to-digital converters (ADCs) for interfacing to these two popular resistive touch screens. Since the majority of applications use 4-wire touch screens, the rest of this article concentrates on this architecture, although the same advice applies to the 5-wire screens and the ADS7845, TI's 5-wire touch-screen controller.

Figure 2. Touch-Screen Circuit Configurations



Resistive touch-screen controllers

When a position is measured on a 4-wire touch screen, voltage is applied across the screen in the Y direction; and a touch presses the layers together, where a voltage can be read from one of the X electrodes. The pressure creates a voltage divider at that point, so the Y coordinate can be determined; the process then repeats with the X direction being driven, and a reading is taken from one of the Y electrodes.

A touch-screen controller is simply an ADC that has built-in switches to control which electrodes are driven and which electrodes are used as the input to the ADC. The ADC can often be operated with different reference modes: single-ended or differential.

Single-ended configuration

In a single-ended configuration, the ADC reference is supplied between a reference input (V_{REF}) and ground. Very often, V_{REF} is actually the power supply voltage. The ADC output is then a ratio of the input signal to the V_{REF} voltage. Since the touch screen is a voltage divider, this may seem sensible. However, there are several possible errors that may show up due to the driver switches, such as gain and offset errors from temperature, voltage drops in the switches, etc. If the reference voltage is not the power supply, then power-supply variations could cause errors, since the power supply is the voltage placed across the screen; and, while it varies, the reference voltage will not. Variations in touch-screen impedance can also cause gain or offset errors.

Differential configuration

In the differential configuration, the ADC's voltage reference is taken directly across the touch screen, eliminating driver variations, power-supply changes, and even changes in the touch-screen impedance. The output of the ADC is still the ratio of the input to V_{REF}. V_{REF} is now the voltage across the screen, and the output is a true reflection of the position of the touch on the screen. Using a differential or ratiometric measurement technique like this provides much more accurate results, particularly in systems with noisy power supplies or where the touch screen is located a significant distance away from the controller.

Touch-screen settling time

When the touch panel is pressed or touched, there are two mechanisms that will affect the voltage level at the contact point. These two mechanisms will cause the voltage across the touch panel to "ring" and then to settle (decay) down slowly to a stable dc value.

The two mechanisms are:

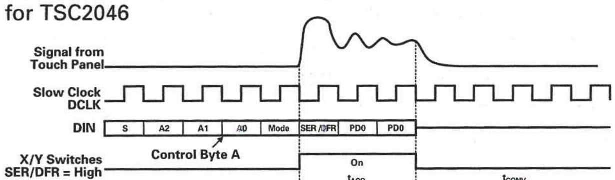
1. Mechanical bouncing caused by vibration of the top layer sheet of the touch panel when the panel is pressed.
2. The charging of the parasitic capacitance between the top and bottom layer sheets of the touch panel and at the input of the ADC that occurs when the drivers turn on, and inductive effects from the leads connecting the panel to the drivers in the controller.

Difference between single-ended and differential modes

In both single-ended and differential modes, the ADC acquires (samples) the input analog voltage from the touch panel for some time, t_{ACQ} (see Figure 3). The input voltage has to settle within t_{ACQ} in order for the ADC to capture the correct voltage.

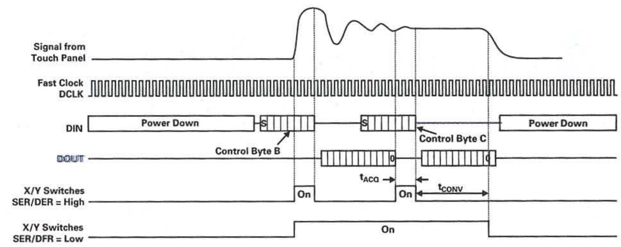
Turning the drivers on causes the touch panel's voltage to rise rapidly and then settle to the final value, as shown in Figure 3. To acquire the correct value for conversion, the acquisition must be complete when the touch panel has completely settled. There are two ways of accomplishing this.

Figure 3. Timing diagram of single-ended-mode operation for TSC2046



One method (shown in Figure 3) uses the ADC in single-ended mode and a relatively slow clock. A slow clock extends the acquisition time, since it extends the clock periods used for acquisition. The drivers turn on at the beginning of the first of three clock periods (for simple controllers like the ADS7843, ADS7846, TSC2003, and TSC2046). The panel must then settle completely during the following two clock cycles, so that at the end of the third clock cycle, the acquired voltage is accurate.

Figure 4. Using a fast clock in differential mode for TSC204

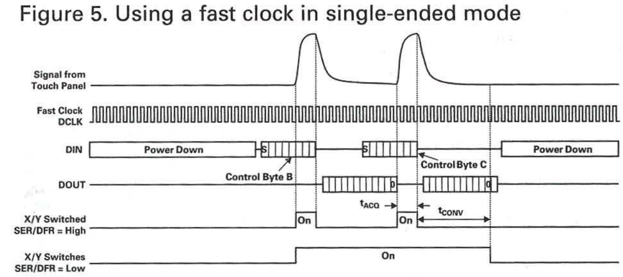


The second method (shown in Figure 4) uses the differential mode and a much faster clock rate. Control byte B turns the drivers on and, as before, the touch panel's voltage rises rapidly and begins to settle. In this case, a conversion is done, and then a second conversion is begun, by sending control byte C. If control bytes B and C are the same, the internal X/Y switch of the ADC will not turn off after completing a conversion for control byte B. Thus, the touch panel voltage will be settled by the time the conversion from control byte C begins, and this conversion will be accurate. This method requires that the conversion result from control byte B be discarded, as it will not be accurate since its acquisition period occurred when the touch panel voltage was still ringing.

An advantage to using the second method is the potential for power savings. After the end of conversion for control byte C, the controller can go into power-down mode and wait for the next sampling period. In the slow clock case, the next sample period may have to come immediately after the current conversion, leaving no time for power down.

Using a fast clock in single-ended mode (Figure 5) would not be of any help, because the drivers turn off between conversions. This results in the touch panel's voltage rising at the beginning of each conversion, which never gives the touch panel a chance to settle.

Figure 5. Using a fast clock in single-ended mode



Making the ADC results usable for a human interface

Since several measurements for one coordinate pair are being taken, the designer has the opportunity to do some processing on this data, like averaging. This will help prevent spurious readings that may make dealing with the human interface difficult.

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BY DAVID ARCINIEGA AND WILL HARRIS • TEXAS INSTRUMENTS

ExpressCard eases power-management woes

ALTHOUGH THE EXPRESSCARD POWER-MANAGEMENT STANDARD IS SIMILAR TO PC CARD TECHNOLOGY, IMPORTANT DESIGN DIFFERENCES EXIST.

An ExpressCard module is an add-in card with a serial interface based on PCI Express, the USB (Universal Serial Bus) technologies, or both. The host system provides power to the ExpressCard slot as the ExpressCard standard specifies. The PCMCIA Committee in the early 1990s developed the PC Card standard (**references 1** and **2**). The committee maintained the PC Card standard's proven methodology for power management during the development of the ExpressCard standard. However, some differences between the implementations exist in both the host and the module. It is important to note that, because the ExpressCard technology applies to both notebook and desktop computers, the host power management for ExpressCard modules is the same for the two platforms.

ExpressCard modules, like PC Cards, receive power through the connector after a user has inserted the card and the host system has detected it. A host system that accepts PC Cards follows the sequence for applying power as the PC Card standard stipulates. This sequence involves the PC Card controller, which resides on the host, monitoring the card-detection and voltage-sense pins on the connector. As their name suggests, the card-detection pins signal the presence or absence of a PC Card in a socket, and the voltage-sense pins inform the PC Card controller of the card's voltage requirements. Upon detecting that a user has inserted a card into the socket, the PC Card controller reads the logic levels on the voltage-sense pins and then sends a command to the PC Card power switch to turn on the corresponding voltages to the module. This command can be either a serial stream or a parallel interface, depending on the type of power switch the application uses.

The PC Card power switch has two voltage-output connections, V_{CC} and V_{PP}, to the module. Depending on the PC Card installed in the socket, the V_{CC} output can be either 3.3 or 5V, and the V_{PP} output can be 1.8, 3.3, 5, or 12V. **Figure 1** shows a typical implementation of a PC Card application. The power switch serves as a multiplexer, sending only the desired voltages to the PC Card.

SIMPLE MANAGEMENT

The developers of the ExpressCard standard simplified the power management in the host. Instead of having the power switch act as a multiplexer, three voltage rails connect to the ExpressCard module. The availability of these voltages to the module is consistent with a PC Card implementation in which the voltages become available only after a user inserts a card into the slot. The use of card-present inputs from the module is also consistent. However, unlike the PC Card implementation, these inputs go directly to the power switch. This approach thus eliminates the use of the PC Card controller, thereby simplifying the design. The ExpressCard power switch now has to detect whether a user has inserted a card into the slot. **Figure 2** shows a typical ExpressCard implementation. Even though the typical implementation looks simpler, the ExpressCard power switch also must decide when to send voltages to the module or which ones to send. The switch makes these decisions based on the state of the host system, which the primary 3.3 and $1.5V_{IN}$ and auxiliary $3.3V_{AUX\_IN}$ voltage rails define.

If both the primary 3.3 and $1.5V_{IN}$ power and auxiliary 3.3_{VAUX_IN} power at the input of the ExpressCard power switch are off, then all output voltages going to the ExpressCard connector are

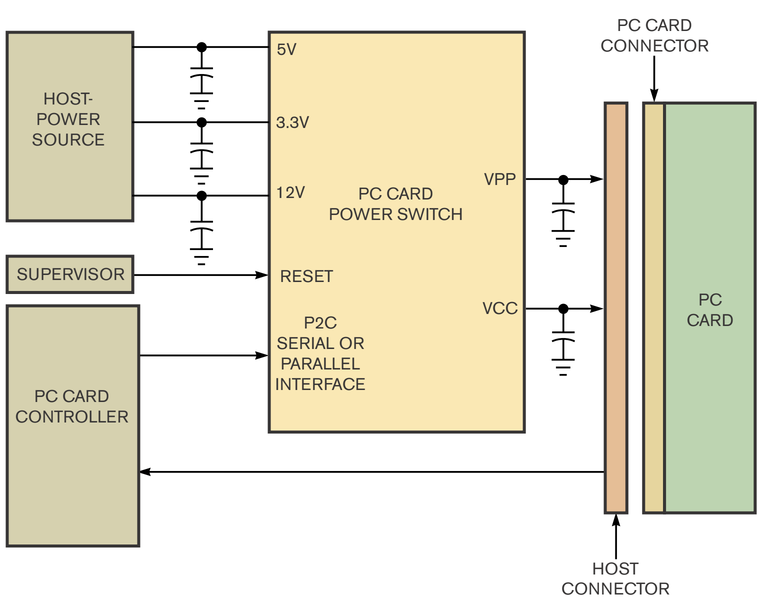

Figure 1 In a typical PC Card application, the power switch serves as a multiplexer, sending only the desired voltages to the plug-in card.

also off, regardless of whether a card is present. Also, if auxiliary power is available and no card is present, all the voltage outputs to the ExpressCard slot must remain off. If both the primary and the auxiliary power are present at the input of the ExpressCard power switch, then power goes only to the ExpressCard slot after the ExpressCard power switch detects that a card is present.

If either 3.3 or 1.5V primary power at the input of the ExpressCard power switch is off and auxiliary power at the input is available, then the ExpressCard power-switch outputs depend on the state of the host system and on the state of the card-present inputs. If no card is present, then no power goes to the ExpressCard slot. If a user inserts the card after the system has entered this power state, then no power goes to the ExpressCard slot. If a user inserts the card before removing the 3.3V primary power, the 1.5V primary power, or both at the input of the ExpressCard power switch, then only the 3.3 and 1.5 primary power shuts off, and the auxiliary power still goes to the ExpressCard slot. In this scenario, the ExpressCard module can wake the system. This approach differs for a PC Card implementation in that, to enable a PC Card to wake the system from a low-power state, a user must supply main power to the PC Card, the PC Card controller, and the associated power switch. To enable an ExpressCard module to wake the system, the user needs to supply only $3.3V_{AUX\_IN}$ to the module. This approach reduces the total power consumption of a system and eases the implementation of wake-up support from an ExpressCard slot versus a PC Card slot.

For ExpressCard implementations, the ExpressCard power switch should use the $3.3V_{AUX\_IN}$ voltage rail for biasing. The ExpressCard power switch cannot operate if $3.3V_{AUX\_IN}$ is unavailable, and, as a result, the ExpressCard power switch still does not provide power on its output, even if the primary-power voltage rails are present.

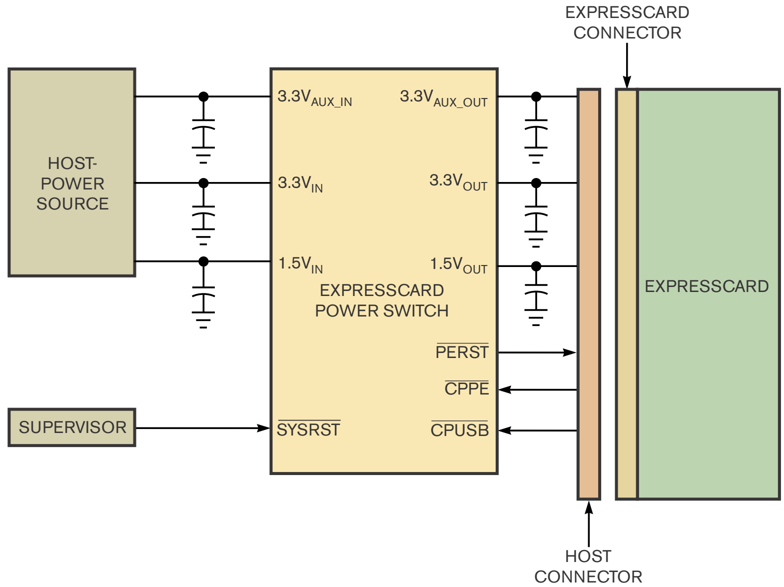

Figure 2 The ExpressCard implementation eliminates the separate card controller by routing card-present signals directly to the power switch.

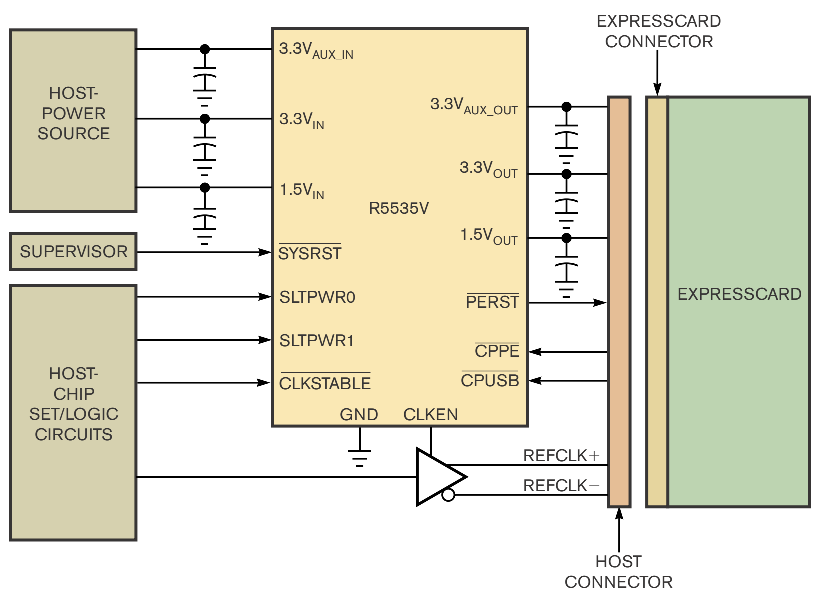

Figure 3 The Ricoh R5535V is an ExpressCard power switch.

The card-present signals $\overline{\text{CPPE}}$ and $\overline{\text{CPUSB}}$ are inputs to the host and to the ExpressCard power switch from the ExpressCard module. They signal the host when a user has inserted a card. The ExpressCard standard requires the host to pull up both of these inputs. The $\overline{\text{PERST}}$ signal is an output from the host; PCI Express-based modules use $\overline{\text{PERST}}$ as a reset signal. It is a power-good indicator such that during power-up and -down and whenever power to the ExpressCard module is unstable or outside voltage-tolerance limits, $\overline{\text{PERST}}$ asserts as the ExpressCard standard requires.

The host can use the $\overline{\text{SYSRST}}$ input to the ExpressCard power switch to place the ExpressCard module in a reset state. Asserting $\overline{\text{SYSRST}}$ automatically generates a $\overline{\text{PERST}}$. Generating a $\overline{\text{PERST}}$ by asserting $\overline{\text{SYSRST}}$ does not disrupt the voltage rails such that it causes the ExpressCard module to perform a "warm" reset. In a "cold"-start situation, $\overline{\text{SYSRST}}$ can also extend the length of time that $\overline{\text{PERST}}$ asserts.

POWER-SWITCH IMPLEMENTATIONS

During the development of the ExpressCard standard, the PCMCIA committee wrote the power-sequencing requirements to allow the designer of the host to implement the approach using discrete components. However, in an effort to save space, major power-switch manufacturers, such as Ricoh, Rohm, and

Texas Instruments (www.ricoh.com, www.rohm.com, www.ti.com), provide integrated approaches. **Figures 3**, **4**, and **5**, respectively, show high-level implementations of each of these approaches. Each of the ExpressCard power-switch implementations differs only in the additional features that each company provides (**references 3**, **4**, and **5**). For example, Ricoh and Texas Instruments both provide a discrete output to enable a clock driver. Rohm and Texas Instruments both provide an overcurrent-status output. All three companies provide a means of using discrete inputs to place the ExpressCard power-switch outputs in a standby state, in which only the $3.3V_{AUX}$ output goes to the ExpressCard. Consult the respective data sheets for a more detailed description of each of these ExpressCard power switches.

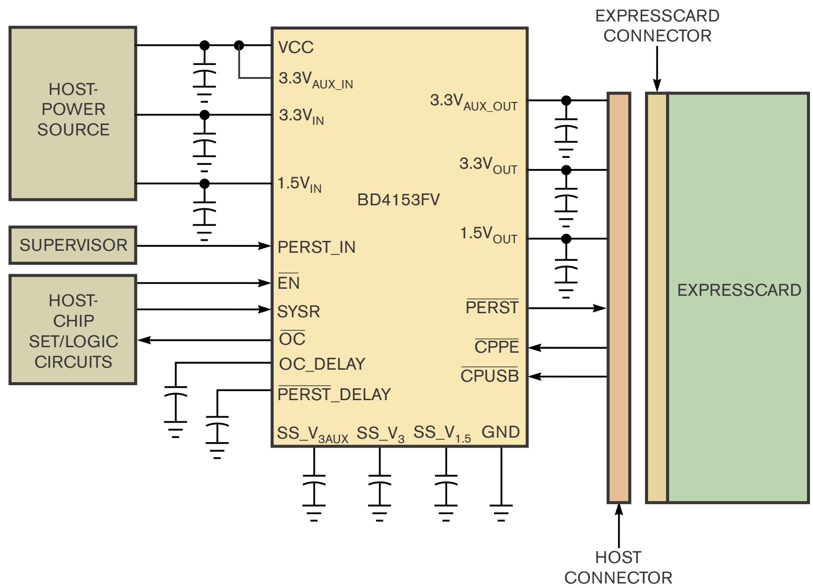

Figure 4 The Rohm BD4153FV switch implements ExpressCard power management.

LINK AND DEVICE STATES

Power management of ExpressCard modules differs depending on whether the module uses a USB or a PCI Express interface. For USB-based ExpressCard modules, the power management is the same as that for a standard USB device that plugs into a USB port. PCI Express-based ExpressCard modules base the power management on the link and device states that the PCI Express base specification defines (**Reference 6**). PCI Express uses the L0, L0s, L1, L2/L3 Ready, L2, and L3 link states to reduce the power consumption of the PCI Express link and, therefore, the PCI Express device on the ExpressCard module. These link states correspond to device states, which derive from PCI power management; CardBus power management also used these link states. PCI Express-based Express Card modules use the same link states for power management. The only difference is that ExpressCard modules require the L1 active state, which is optional in the PCI Express base specification.

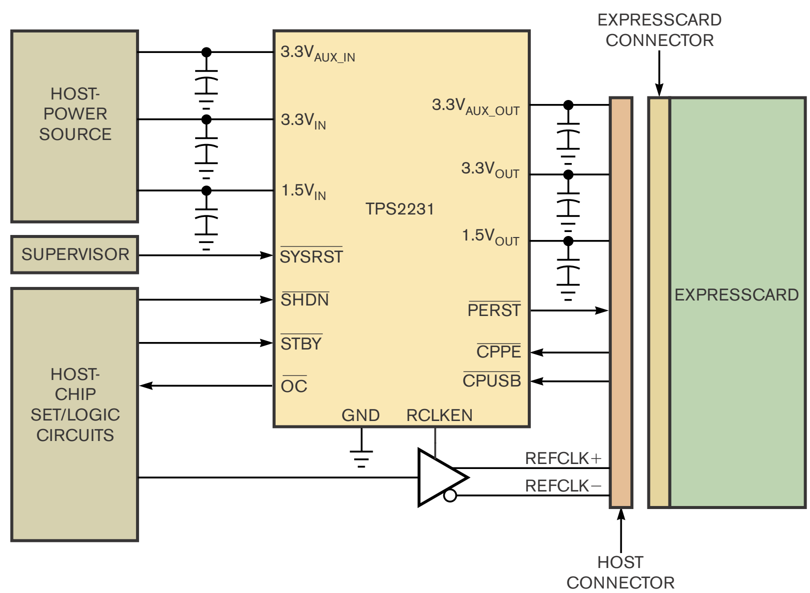

Figure 5 This implementation uses Texas Instruments' TPS2231 ExpressCard power switch.

One way for PCI Express-based ExpressCard modules to maximize power management is to monitor how quickly the module enters the L0s and L1 active states. The faster a module enters these low-power states, the more power savings designers can realize. However, they must consider a performance trade-off: If the modules too quickly enter these low-power states, then the data-transfer rates decrease due to the latency necessary to exit the low-power states. The resolution to this trade-off differs based on the application and desired performance of the ExpressCard module. For example, a PCI bridge allows an ExpressCard module to use legacy PCI-based devices. In such a device, a designer could program the PCI Express-to-PCI bridge to enter the L0s active state almost immediately following a PCI Express transaction. Due to the relatively small amount of time to move from the L0s to the L0 state, the performance of the module would remain the same. Using the same device, a designer could adjust the L1 active-state entry time to be slightly longer than the time between back-to-back PCI transactions. This approach allows for maximum performance from the ExpressCard module when data is transferring but allows for quick entry into the L1 active state and maximum power savings when no data is transferring.

Like CardBus cards, PCI Express-based ExpressCard modules also use device states for power savings. These device states, D0, D1, D2, D3hot, and D3cold, allow for software to direct the

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module to enter a low-power state. The PCI Bus Power Management Interface Specification describes these device states. When in a low-power state, ExpressCard modules can use techniques such as clock gating to turn off inactive portions of the module, thus reducing power consumption.

Another aspect of power management for ExpressCard modules is the presence of a 3.3V auxiliary supply in addition to the 3.3 and 1.5V main supplies. An ExpressCard module can leverage the auxiliary supply to segment the power management and wake-up logic from the rest of the logic in the module. Then, when someone removes main power and the ExpressCard module enters a low-power state, only the power management and wake-up logic remain on. The core logic in the module remains off, greatly reducing power consumption, yet the module retains the ability to wake the system. The PC Card standard includes no auxiliary power supply. As a result, the same supply in a PC Card powers all of the logic, preventing a significant power reduction when the PC Card is in a low-power state.

Though based upon the proven power scheme in the PC Card standard, the ExpressCard standard provides a more robust power-management methodology. On the host side, designers can implement ExpressCard power control without the dedicated controller that PC Cards need. On the module side, link states allow modules to enter low-power states, and a separate 3.3V auxiliary supply eases the implementation of wake-up support. These features enable an ExpressCard system to not only meet, but also improve upon the power savings designers can realize with a PC Card system.

AUTHORS' BIOGRAPHIES

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Will Harris is a systems engineer and member of the group technical staff at Texas Instruments, where he currently works in the computer-connectivity-solutions group. He holds a bachelor's degree in electrical engineering from Texas A&M University. **EDN**

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I^{2}C Bus Buffers

High Performance Analog Solutions from Linear Technology

The I^{2}C bus was originally developed to provide a communication link between integrated circuits within a given system. Over time, the bus became generally accepted in the industry as the de facto standard for chip-to chip communications, and soon thereafter stretched across multiple boards inside a closed system. Modern network servers, telecom switches, computing systems and embedded controllers for industrial applications all employ the I^{2}C bus to link multiple internal devices together.

The growth in number and complexity of plug-in boards and input/output (I/O) cards imposes extensive remote system management and control needs for servers via I^{2}C. The expansion of systems and hence the communication bus has naturally opened the door to unanticipated new problems and issues. Recognizing the need to solve these common problems and simplify systems design utilizing the I^{2}C bus, Linear Technology developed solutions that overcome the basic problems.

The LTC4300 family allows the user to plug I/O cards into a live backplane without corrupting the data transaction on the backplane. The device provides bidirectional capacitance buffering for I^{2}C busses connected across the backplane. As a result, the backplane bus sees only the capacitance of the buffer ICs (less than 10pF each) instead of entire cards' bus capacitance. This dramatically increases the number of nodes that can be supported in a given system and improves signal integrity. It also makes the family ideal for any I^{2}C-based system, allowing for the addition of many more devices to a single bus than previously possible.

Expanding on the existing family of I^{2}C buffers, Linear Technology introduces bus buffers that provide stuck bus recovery and bus multiplexers that feature capacitive isolation.

I^{2}C Bus Buffers with Stuck Bus Recovery

Occasionally, a fault will occur and cause the I^{2}C bus to be stuck low, and the entire system must wait indefinitely. That is a common issue for systems with I^{2}C busses and people have attempted numerous techniques to address this problem.

Common I^{2}C Problem	LTC4300 Family Solution
Maximum 400pF Capacitive Loading	Capacitive Isolation
Strong Pull-Ups, Slow Rise Time	Rise Time Accelerator
Live Insertion of New Devices	Performs Hot Swap Function
Different Voltage Levels	Voltage Level Translation
NEW Stuck Bus	Stuck Bus Detection and Recovery
Bus Switching and Address Expansion	Multiplexers with Capacitive Isolation

LINEAR TECHNOLOGY

I²C Bus Buffers

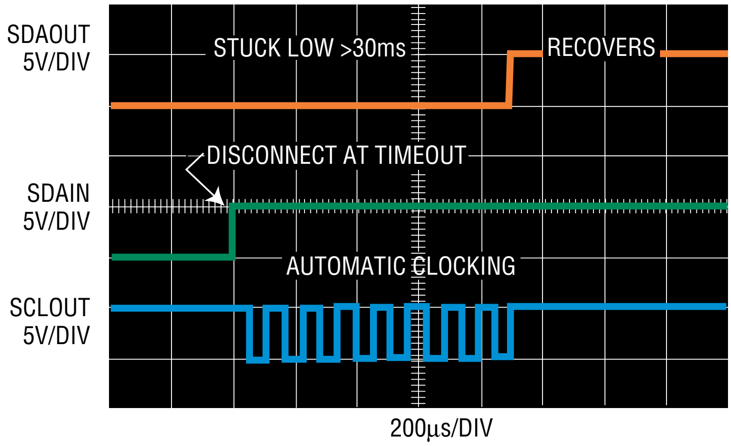

Figure 1. LTC4303/LTC4304 I²C Bus Buffers with Stuck Bus Recovery

The LTC4303 and LTC4304 are 2-wire bus buffers with stuck bus recovery. These new chips solve the problem by isolating the upstream side, while restoring the downstream one. If the serial data output (SDA) or serial clock output (SCL) are low for more than 30ms, the LTC4304 will automatically break the data and clock bus connections and issue a Fault signal. Sequentially, the parts will automatically generate up to

Figure 2. I²C Multiplexers

sixteen clock pulses on the SCL in an attempt to free the bus. When the bus becomes free, a connection will be immediately enabled and proper operation will resume. With stuck bus recovery, the LTC4303 and LTC4304 eliminate the need for a general system reset and unburden the microcontroller, providing the appropriate signals to free the bus.

The LTC4303 and LTC4304 also provide capacitive isolation between the backplane and the card's I²C busses, even if their respective supplies are at different levels. The ICs perform this level translation without the need for a second supply pin or a second pair of input pull-up resistors, eliminating the need to dedicate a connector pin for the backplane supply voltage.

The LTC4303 is offered in MSOP-8 and 3mm x 3mm DFN packages and is pin-compatible with the LTC4300A-1. The LTC4304 is available in MSOP-10 and 3mm x 3mm DFN packages.

I²C Multiplexers with Capacitive Bus Buffering

I²C multiplexing allows for reliable switching of multiple system management buses and multiple I²C devices, while also solving common addressing problems.

The LTC4305 and LTC4306 are 2-wire bus multiplexers that also provide vital capacitive isolation while connecting an upstream bus to a desired combination of downstream busses. Software controlled, the LTC4305 multiplexes two channels, whereas the LTC4306 splits the I²C bus into four sub-branches.

I²C multiplexing also allows for address expansions as well as for addressing one of multiple identical devices, thus resolving address conflict issues. Some devices, such as certain temperature sensors and Small Form Factor Pluggable (SFP) modules, have only one I²C address and in many cases several of these identical devices are needed within the system. In Figure 3 below, the LTC4305 connects to two SFP modules with identical device addresses. If both modules were plugged directly into the backplane, they would require two unique addresses. However, if the master uses the LTC4305 in multiplexer mode, where only one downstream

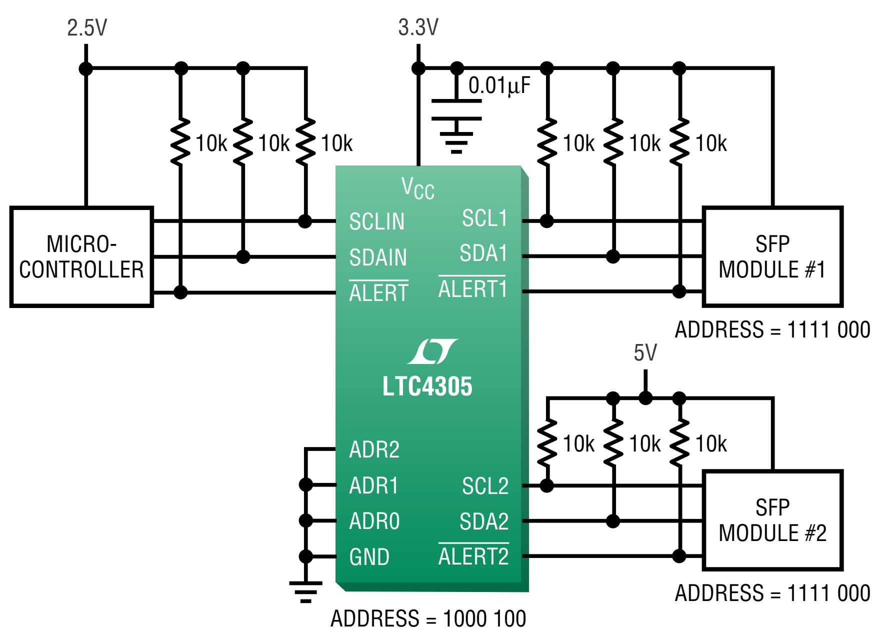

Figure 3. Level Shifting and Nested Addressing Circuitry

I²C Bus Buffers

channel is connected at a time, then each module can have a device with the same address and no problem will occur. The LTC4305 and LTC4306 are also useful in systems that have multiple identical I/O cards, having addresses that are hardware programmed upon insertion into a backplane by fixed pins. Both ICs allow for 27 distinct bus addresses that are configurable by using the three 3-state address pins.

Many I²C devices operate at different voltage levels, yet they must share the common bus. The LTC4305 and LTC4306 are supply independent. Therefore, each channel can be pulled to a supply voltage ranging from 2.2V to 5.5V regardless of the ICs' supply voltage. Again, this level translation is performed without the need of a second supply pin or a second pair of input pull-up resistors.

The LTC4305 and LTC4036 offer additional key features. Downstream channels are provided with two (LTC4305) and four (LTC4306) alert inputs for fault reporting. Should a stuck bus be detected, a programmable timeout circuit will automatically break the data and clock bus connections, issuing an alert. The ICs, however, do not attempt to generate clock pulses to recover the stuck bus.

When activated, the rise time accelerator circuit sources currents into the 2-wire bus pins, which reduces the time needed to reach proper bus levels and overcome heavy capacitive loads. The LTC4306 also features two general purpose input/output (GPIO) pins that can be configured as inputs, open-drain outputs, or push-pull outputs.

The LTC4305 is available in 16-lead SSOP and 4mm x 5mm DFN packages. The LTC4306 is available in 24-lead SSOP and 4mm x 5mm QFN packages.

Table 2. Linear Technology's Bus Buffer Products

I²C Products	LTC Part Number	Enable Input	Ready Output	Level Shifting	Comments
Bus Buffers	LTC4300A-1	✔	✔		MSOP
	LTC4300A-2		✔	V_{CC} Pins	MSOP
	LTC4300A-3	✔		V_{CC} Pins	DFN 3mm x 3mm, MSOP
Supply Independent Bus Buffers	LTC4301	✔	✔	Auto	DFN 3mm x 3mm, MSOP
	LTC4301L	✔	✔	Auto	Accepts Voltages as low as 1V
Addressable Bus Buffers	LTC4302-1	✔	✔		32 Possible Addresses, 2 GPIOs
	LTC4302-2	✔	✔	V_{CC} Pins	32 Possible Addresses, GPIO
Bus Buffers with Stuck Bus Recovery	LTC4303	✔	✔	Auto	Pin-Compatible with LTC4300A-1
	LTC4304	✔	✔	Auto	Fault, Accelerator Disable
Bus Multiplexers with Capacitive Buffering	LTC4305	✔	✔	Auto	2-Channel Mux, 27 Distinct Addresses
	LTC4306	✔	✔	Auto	4-Channel Mux, 27 Distinct Addresses

BY IAN FERGUSON • QUICKLOGIC

Architectural-design considerations for implementing hardware acceleration

EXPLOITING HYBRID SOFTWARE/HARDWARE PARALLELISM IN ALGORITHM-HARDWARE ACCELERATIONS CAN YIELD SIGNIFICANT PERFORMANCE GAINS OVER A FUNCTION-REPLACEMENT APPROACH.

Across a range of embedded-system applications, the combination of data-processing and system-throughput requirements is increasing to the point at which implementing algorithms purely in software on a single high-powered CPU is exposing two challenges. First, system power and cost are forced upward. Besides the obvious battery-life issues that exist for mobile platforms, rising power dissipation increases the requirement for heat sinks and supplemental cooling. Second is the issue of implementing value-added functions to a system when handling the baseline system functions fully occupies the CPU's processing capacity—especially when a designer cannot implement the new functions without including additional components.

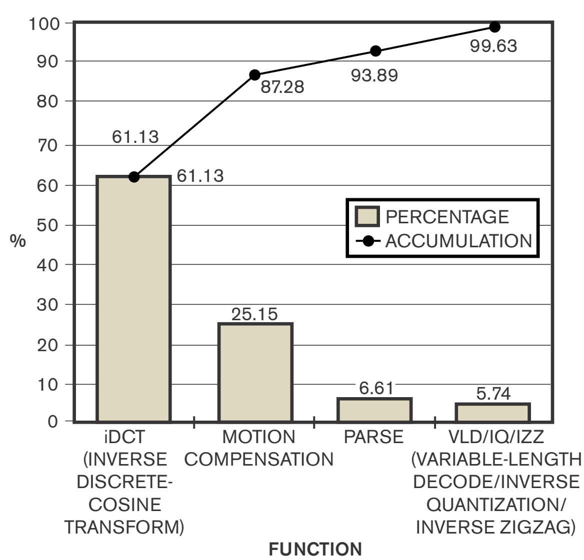

Figure 1 Grouping the individual functions for MPEG-2 decoding according to high-level function produces a histogram that summarizes the percentage of execution time by function and shows their aggregated percentage of the complete algorithm.

What options are available? For the purposes of this article, the choices break down into three areas. Customizing the CPU's instruction set for the application can markedly improve algorithm-processing efficiency. The usability of development tools for harnessing such cores continues to significantly improve over that of a few years ago. This strategy could potentially bind a designer to a specific implementation that can over time cause legacy-software issues.

If a designer can segment an application into well-defined, somewhat-independent tasks, then using multiple CPU cores can improve the algorithm-processing efficiency. Unless the application design has the volumes to justify an ASIC development, the only viable options for this approach are using proprietary CPU cores in FPGAs or finding an ASSP (application-specific standard processor) that exactly meets the desired system requirements.

Another option, which is the focus of this article, is for the designer to migrate performance-hungry elements of the algorithm into hardware; the implementation could be as an ASIC, a structured ASIC, an ASSP, or an FPGA. To illustrate the process and the challenges associated with this approach, this article draws from a QuickLogic (www.quicklogic.com) project that involved constructing an MPEG-2 decoder as a hybrid combination of hardware and software modules on a programmable SOC (system on chip). Although the results are specific to the MPEG-2 decoder, the process and the system-design considerations apply to a broad set of embedded-system applications.

The first step is to identify elements of the algorithm that are suitable for accelerating. To accomplish this task, it is necessary to understand the areas of the code base in which the microprocessor is spending most of its time. You achieve this step by profiling the code. Although the insertion of profiling code can slow and intrusively affect the application performance, it will, as a first approximation, locate the main hot spots in the code. Indeed, newer Linux kernels are starting to build in profiling support that will significantly reduce this problem.

The project team used a GNU-C compiler to build special statistics-measuring code into the binary executables. A program built with profiling support generates a gmon.out file that contains statistics it gathers while the program is running. The gprof utility, which interprets the gmon.out file, generates text files that indicate how many times a function executed and the overall time spent in a function.

Grouping the individual functions for MPEG-2 decoding according to high-level function produces a histogram that summarizes the percentage of execution time by function and shows their aggregated percentage of the complete algorithm (**Figure 1**). For the MPEG-2-decoding algorithm, the top four elements comprise more than 99% of execution time.

HARDWARE IMPLEMENTATION

On its own, a hardware-accelerator block simply takes data in, processes it, and then outputs the result. A particular system environment requires interfaces for the data to feed the accelerator. This module therefore needs to include an interface to the on-chip or external bus where the CPU is located and a DMA engine to feed data into and out from the accelerator block.

Replacing a software function (such as iDCT shown in **Figure 1**) that takes 61% of a microprocessor's time with hardware does not translate into a 2.5-times performance improvement. This scenario is primarily because of the communication overhead between the CPU core and the hardware-accelerator block as well as the efficiency of the storing/retrieval process of data from memory and the location of data in the system.

Systems employing only software for algorithm implementations typically spend most of their time executing mathematical operations within the core algorithm. When you express those core algorithms in hardware, the CPU acts as more of a controller, coordinating and scheduling the operations of the hardware accelerator. Typically, you accomplish this task by setting up DMA operations, configuring register bits, and placing instructions into command queues.

As an example, assume there are three transforms: T1, T2, and T3. Suppose that T1 and T3 each consume 30% of the CPU time and that T2 consumes only 1%. When T1, T2, and T3 pass significant amounts of data between them, excluding T2 from the acceleration may significantly impact the performance beyond what the 1% profiling may indicate.

Suppose that each transform function reads 1 kbyte of data and then writes back 1 kbyte of data. If T1 and T3 are hardware implementations, and T2 is a software implementation, the data flow will result in 6 kbytes of data traffic (**Figure 2a**). You cannot base your prediction of the resulting performance on the profile data because the exclusion of T2 creates additional system-data movement. As an alternative, you can implement all three transforms in hardware and localize the data transfer between T1/T2 and T2/T3 within the hardware accelerator (**Figure 2b**); the result is that only 2 kbytes of data traverses the system bus.

In the case of the histogram for the MPEG-2 decoder, after the iDCT and motion-compensation functions, the parse function is the next logical candidate for hardware acceleration. However, due to the data flow of the algorithm, accelerating parse without the acceleration VLD/iQ/iZZ (variable-length decode/inverse quantization/inverse zigzag) is likely to create the problem of data localization. Therefore, VLD/iQ/iZZ proves to be a better candidate for acceleration.

ACHIEVING CONCURRENCY

The most straightforward method of partitioning software into a hardware/software hybrid is the creation of a hardware block that exactly mimics the operation of a software function call. This process, function replacement, minimizes the impact on the software because there is no need to redesign the software's upper layers. Additionally, the designer implementing the hardware implementation needs no substantial or intimate knowledge of the algorithm.

This approach does not, however, deliver the highest level of system performance and power improvement, because the CPU core remains idle while the hardware accelerator is processing, and only one hardware block is active at a time. Additionally, the data flow is less than optimal, because each function block must communicate back to the system memory rather

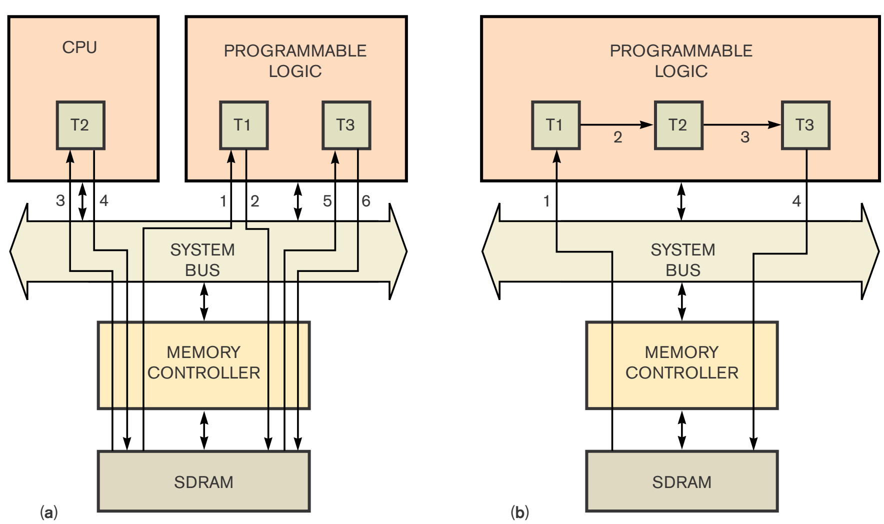

Figure 2 In a data flow with T1 and T3 implemented in hardware, T2 creates additional system-data movement (a). Implementing all three transforms in hardware and localizing the data transfer between T1/T2 and T2/T3 within the hardware accelerator results in only 2 kbytes of data traversing the system bus (b).

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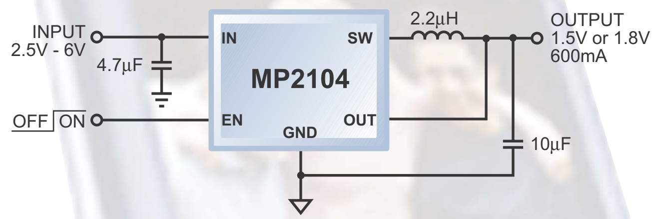

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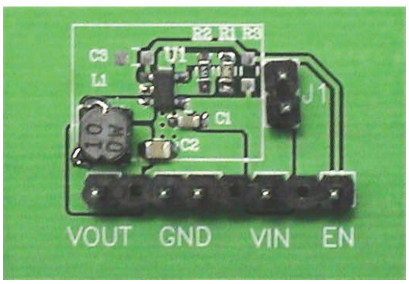

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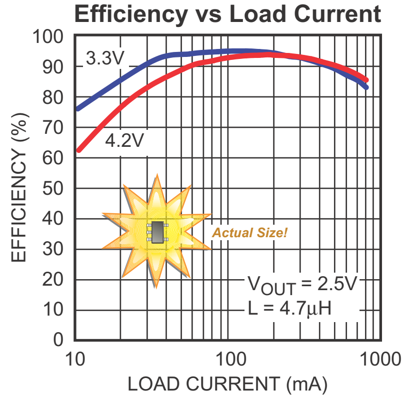
Part	Frequency	V_{IN} (V)	I_{OUT} (A)	Package
Featured Synchronous Bucks				
MP2104	1.7MHz	2.5 - 6	0.6	TSOT23-5
MP2109*	1.0MHz	2.5 - 6	2x 0.8	QFN10 (3x3)
MP2106	800kHz	2.6 - 13.5	1.5	QFN10 (3x3)
MP2305	340kHz	4.75 - 23	2.0	SOIC8
MP1570	340kHz	4.75 - 23	3.0	SOIC8
Featured Non-Synchronous Bucks				
MP2361	1.4MHz	4.75 - 23	2.0	QFN10 (3x3)
MP2364*	1.4MHz	4.75 - 23	2x 1.5	TSSOP20
MP2354	380kHz	4.75 - 23	2.0	SOIC8
MP1593	385kHz	4.75 - 28	3.0	SOIC8

** Dual Output*

MP2104
Efficiency vs Load Current



DC to DC Converters | CCFL / LED Drivers | Class D Audio Amplifiers

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than follow a direct block-to-block communication. This approach therefore is most effective when you apply it to self-contained functions that perform a lot of processing on a small amount of data.

Designers can achieve higher system performance by executing elements of the algorithm concurrently in parallel. For this project, the team identified and considered three device architectures for concurrency. CPU and hardware-accelerator concurrency consists of both systems operating simultaneously. It can occur when the CPU core initiates hardware operations as soon as dependent data is in place and can perform tasks when the hardware accelerator is computing. Concurrency can also occur through the use of multiple hardware-accelerator blocks; this form requires the designer to use acceleration blocks that can execute independently of each other.

Finally, the design can use concurrency within a hardware-accelerator block. Partitioning algorithms as a pipeline of operations can be beneficial to building the hardware as a pipeline of operations that perform concurrently. This approach may require intermediate buffering of data to account for different pipeline stages requiring a different amount of time to complete and ensuring the synchronization of data for use by subsequent execution units.

A challenge to implementing concurrency is the additional engineering effort and knowledge of the algorithm that the designer must have. A number of industry-standard tools offer various levels of automation for function replacement, including Mentor's (www.mentor.com) Seamless profiling tool and ASAP hardware-conversion products, as well as offerings from Coware (www.coware.com), Celoxica (www.celoxica.com), and Critical Blue (www.criticalblue.com). If the function-replacement strategy delivers the necessary performance and power, these tools significantly reduce the effort required to deliver a hybrid implementation. Mentor's tools, for example, assist in the development of the hardware wrapper required for the accelerator and rewrite the software driver to use the hardware accelerator. However, these tools struggle with the development of concurrent implementations.

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In these cases, developing an optimized implementation requires significant investment from individuals that understand the device architecture and the intricacies of the algorithm. This additional effort is justifiable only if the function-replacement approach cannot meet the required performance or power improvement.

The QuickLogic MPEG-algorithm project experienced a 100% system-performance improvement over the function-replacement approach by performing the extra effort to create an application-specific hardware module (**Figure 3**). Overall, the hardware/software implementation provided more than 10 times the performance of a software-only implementation. Additionally, when considering an implementation with no net increase in power dissipation, the system performance experienced a fivefold increase. Clearly, though, the additional performance improvement possible depends on the algorithm.

From this work, our key conclusion is that the magnitude of the performance gain that a designer can achieve using a hybrid implementation depends on two primary elements. The designer needs to understand the nature of the algorithm's characteristics to enable a migration of software to hardware without introducing time-consuming data transfers between modules. Also, for those willing to devote the time to exploit or introduce parallelism inside an algorithm, significant performance gains are possible over a function-replacement approach. The limitation of the off-the-shelf tools to help with this more involved task means that this method requires a significant investment in resources to invoke concurrent processing in the CPU core and the hardware-acceleration logic. EDN

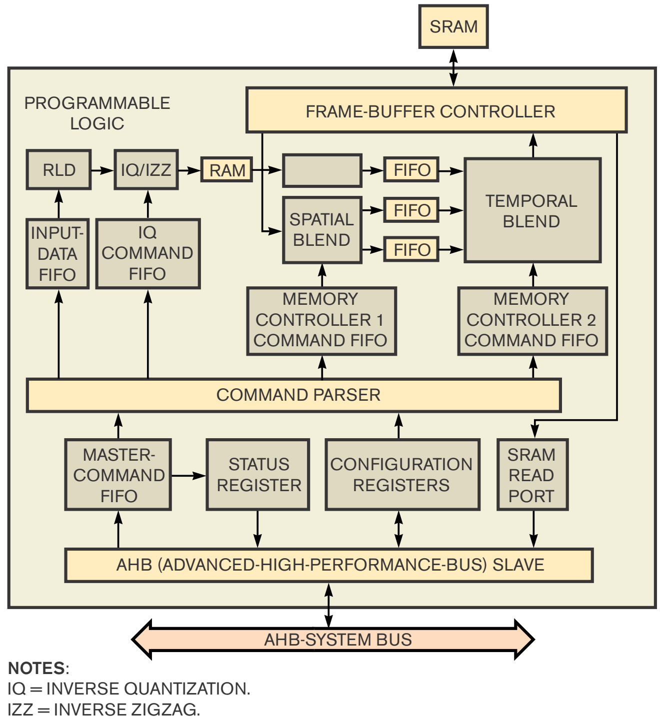


Figure 3 The QuickLogic MPEG-algorithm project experienced a 100% system-performance improvement over the function-replacement approach by performing the extra effort to create an application-specific hardware module.

AUTHOR'S BIOGRAPHY

Ian Ferguson manages QuickLogic's division of Embedded Standard Products devices, including QuickMIPS. The division focuses on defining next-generation devices in partnerships with complementary-silicon suppliers, such as Intel, Renesas, and Atheros. Ferguson has a bachelor's degree in electrical and electronics engineering from Loughborough University (UK). You can reach him at iferguson@quicklogic.com.

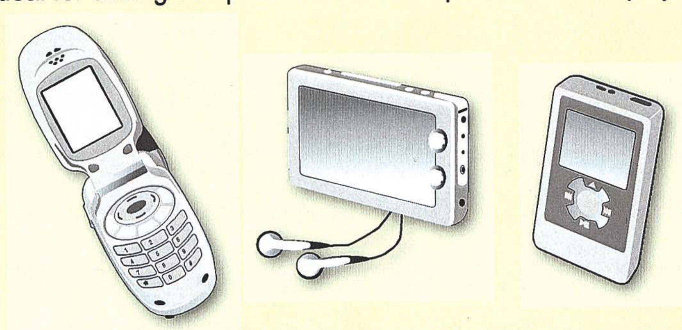
World's Smallest Video Driver

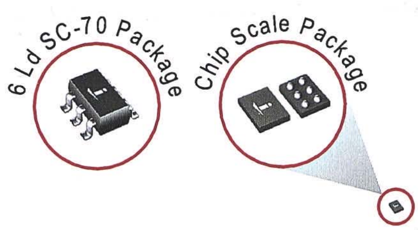
ISL59110 and ISL59111 8MHz rail-to-rail composite video drivers meet the high demands of micropower and bandwidth in battery-operated applications

Space Efficient Package

Available in Pb-Free Package

Ideal for driving composite video out in portable media players





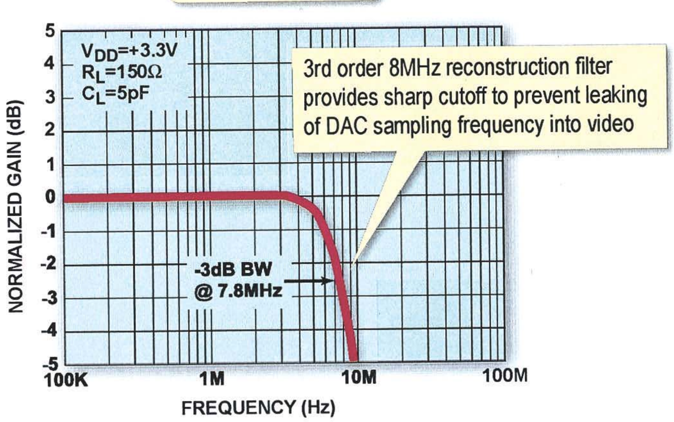
Actual Size
1mm x 1.5mm

Key Features:

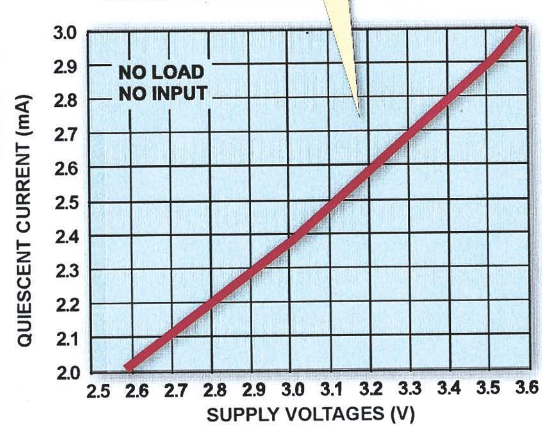
- Available in SC-70 package or smallest 1mm x 1.5mm chip scale package
- Low supply current of 2mA and power-down current of less than 3µA saves battery life

Slew rate of 40V/µs

Low power consumption – operates from +2.5V to +3.6V with an ultra-low 2mA quiescent current



GAIN vs FREQUENCY -3dB POINT

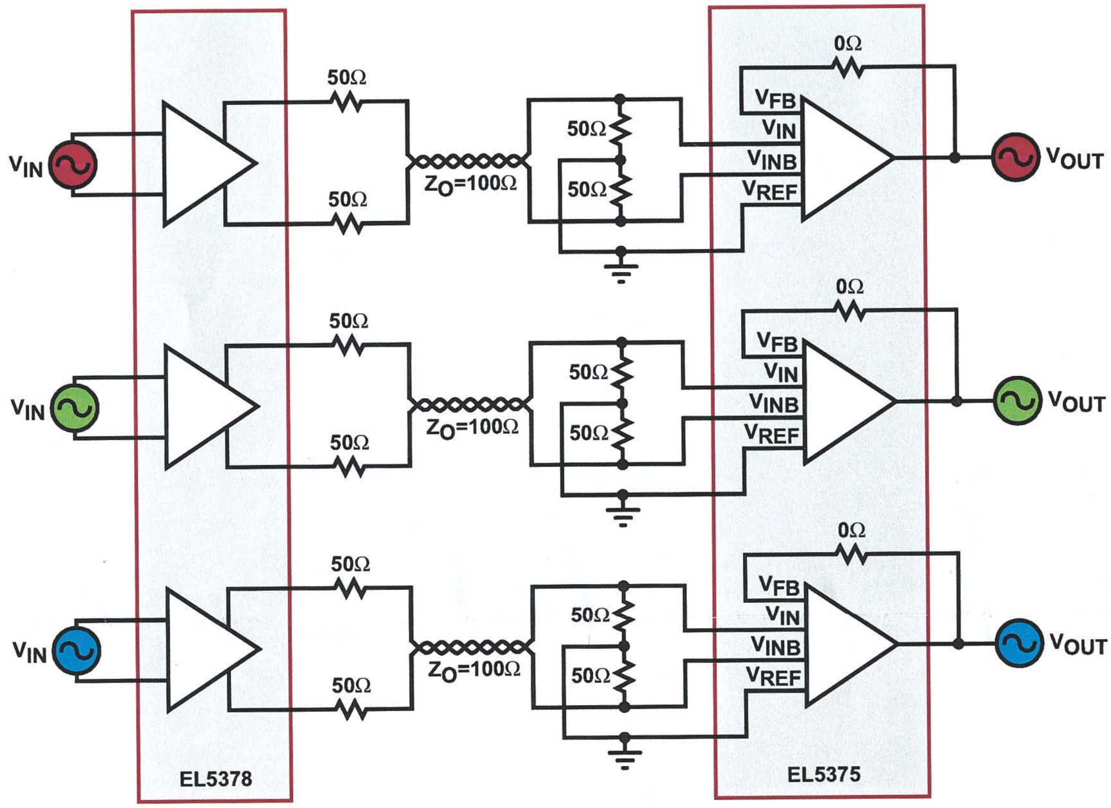


SUPPLY CURRENT vs SUPPLY VOLTAGE

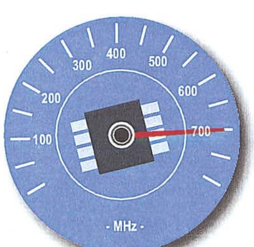
World's Fastest Triple Differential Driver

EL5378 (EL5178) 700MHz Differential Twisted-Pair Drivers

Fixed gain version shown
Programmable gain version available



Receiver feedback resistors are external



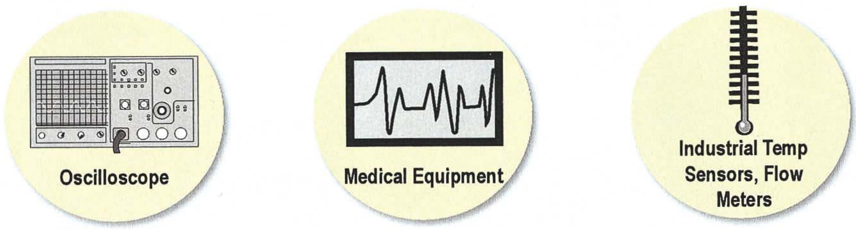
700MHz

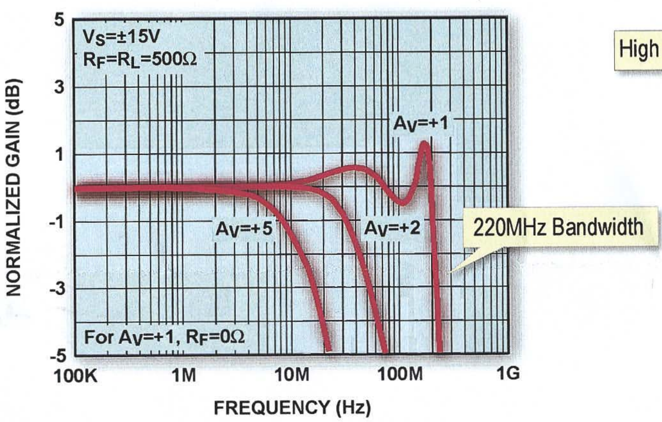
Key Features:

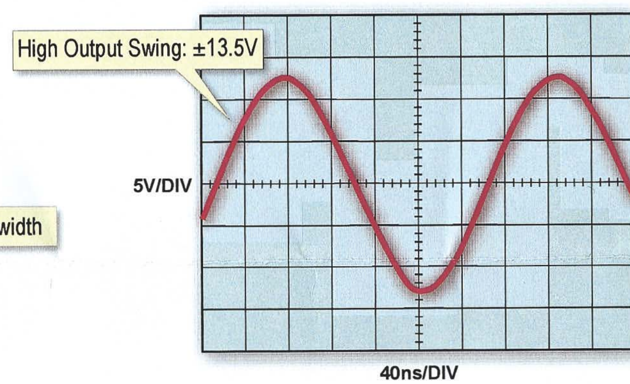
- Fully differential inputs, outputs, and feedback
- Differential input range ±2.3V
- 700MHz 3dB bandwidth
- 1000V/µs slew rate
- Low distortion at 5MHz
- Single 5V or dual ±5V supplies
- 60mA maximum output current
- Low power - 12.5mA per channel

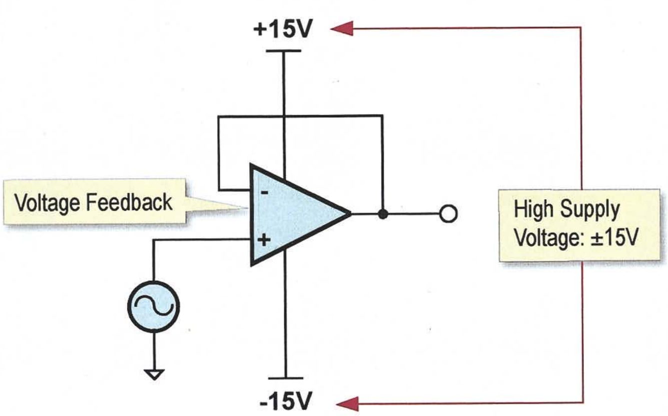
World's First 30V, >200MHz Quad Voltage Feedback Amplifier

ISL55002 and ISL55004 high voltage unity-gain stable op amps







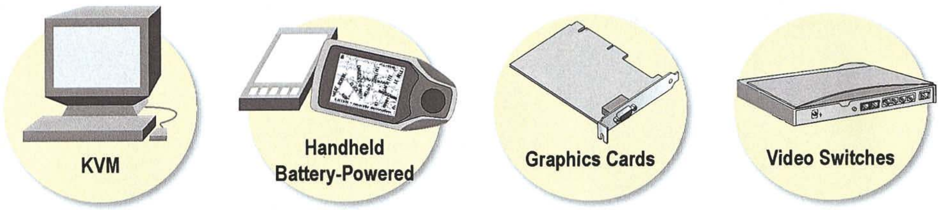


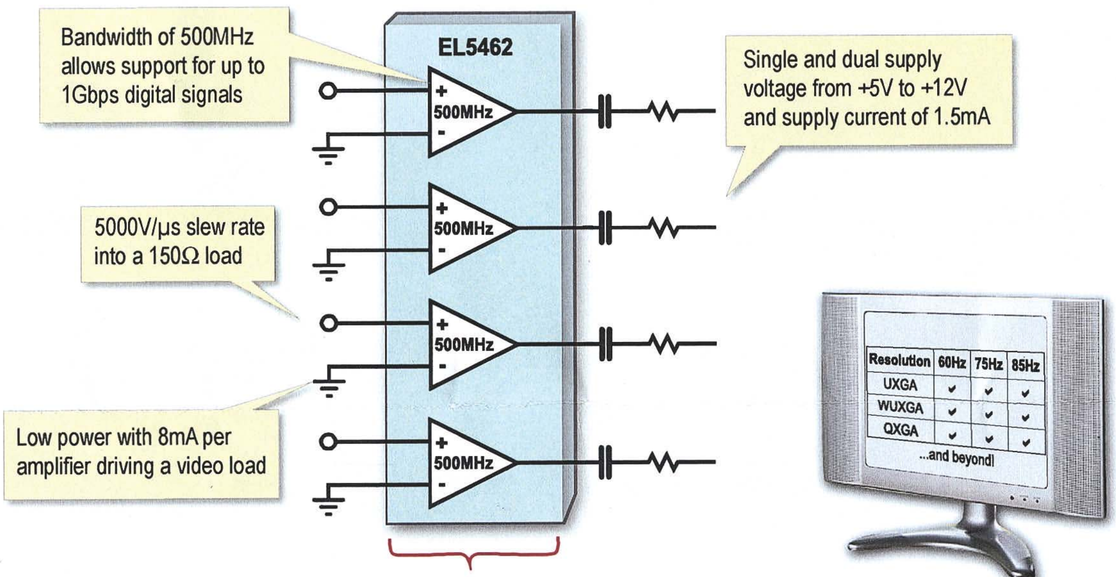
Key Features:

- 220MHz -3dB bandwidth
- Unity-gain stable
- Wide output swing
- Low supply current: 9mA @ V_S = ±15V
- Wide supply range: ±2.5V to ±15V (dual supply) and 5V to 30V (single supply)
- High slew rate: 300V/µs
- Fast settling: 75ns to 0.1% for a 10V step

Low Power Quad Current Feedback Amplifier Drives Resolutions Beyond QXGA

Available in Pb-Free Package





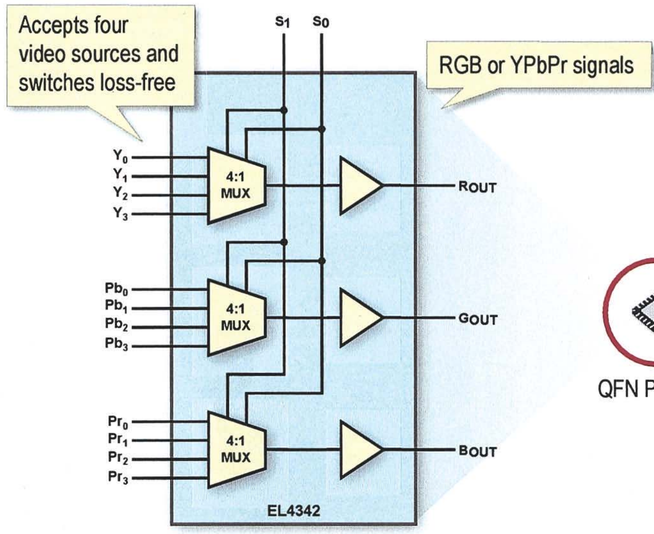
Integrates 4 ultra-fast amplifiers onto a single IC for space-constrained applications

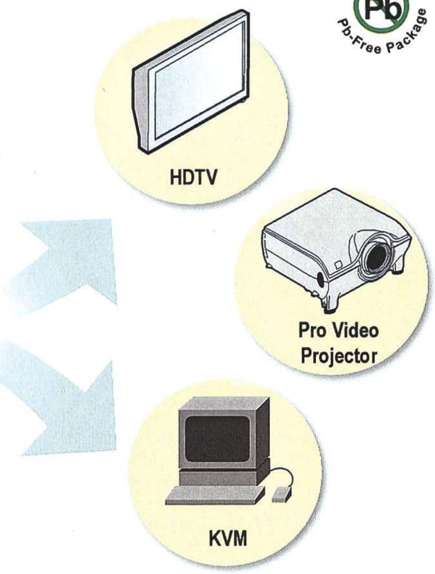
Video Amplifiers - High Speed (>50MHz)

Device	# of Amps	BW @ -3dB (MHz)	Slew Rate (V/µs)	V_S (min) (V)	V_S (max) (V)	V_N (nV/√Hz)	Gain A_V (min) (V)	I_S (per amp) (mA)	I_{OUT} (mA)	V_{OUT} (V)	V_{OS} (max) (mV)
EL5160, EL5161	1	200	1700	±2.5	±5.5	4	1	0.75	70	±3.4	5
EL5260, EL5261	2	200	2000	±2.25	±6.6	4	1	0.75	70	±3.4	5
EL5360	3	200	1700	±2.25	±6.3	4	1	0.75	70	±3.4	5
EL5162, EL5163	1	500	4000	±2.5	±5.5	3	1	1.5	100	±3.6	5
EL5262, EL5263	2	500	2500	±2.25	±6.6	3	1	1.5	100	±3.6	5
EL5362	3	500	2500	±2.25	±6.3	3	1	1.5	100	±3.6	5
EL5462	4	500	4000	±2.5	±5.5	3	1	1.5	100	±3.75	1.5
EL5164, EL5165	1	600	4700	±2.5	±5.5	2.1	1	3.5	140	±3.8	3.5
EL5364	3	600	4200	±2.25	±6.3	2	1	3.5	140	±3.8	5
EL5191	1	1000	2800	±2.25	±5.5	3.8	1	9	120	±3.7	15
EL5367	3	1000	5000	±2.25	±5.5	1.7	1	8.5	160	±3.8	5
EL5166	1	1400	6000	±2.5	±5.5	1.7	1	8.5	160	±3.8	5

1GHz Component Video MUX

ISL59445 1GHz Triple 4 x 1 Multiplexing Amplifier





Available in Pb-Free Package

Key Features:

- Set to gain-of-1 (fixed)
- High-speed 3-state outputs
- Power-down mode
- ±5V operation
- 1GHz -3dB bandwidth
- QFN packaging

Video MUXes with Integrated Op Amps

Device	Configuration	BW @ -3dB (MHz)	SR (V/µs)	I_S (V)	Gain A_V (min) (V)	I_{OUT} (mA)	Diff Gain (%)	Diff Phase (°)	Package
ISL59420	2 to 1	500	900	5	1	100	0.05	0.05	10 Ld MSOP
ISL59440	4 to 1	500	900	7	1	100	0.05	0.05	16 Ld QSOP
ISL59421	2 to 1	1000	1500	10	1	100	0.05	0.05	10 Ld MSOP
ISL59441	4 to 1	1000	1500	14	1	100	0.05	0.05	16 Ld QSOP
EL4340	Triple 2 to 1	500	900	11	1	100	0.05	0.05	24 Ld QSOP
EL4342	Triple 4 to 1	500	900	16	1	100	0.05	0.05	32 Ld QFN
ISL59424	Triple 2 to 1	1000	1500	22	1	100	0.05	0.05	24 Ld QFN
ISL59445	Triple 4 to 1	1000	1500	32	1	100	0.05	0.05	32 Ld QFN

Switches

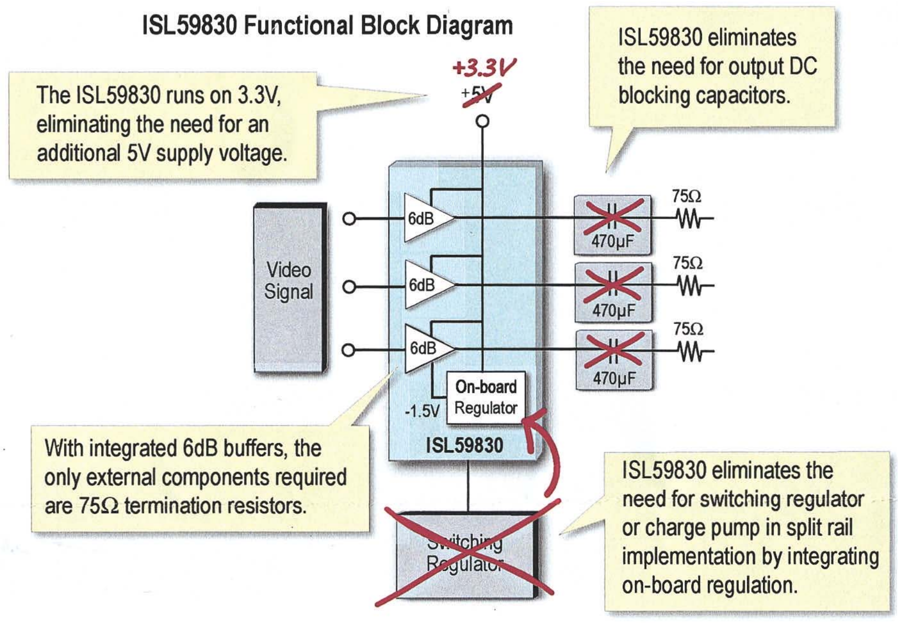
Device	Configuration	R_{ON} @ 5V (Ω)	$T_{(ON)}$ (ns)	$T_{(OFF)}$ (ns)	BW @ -3dB (MHz)	Off Cap (pF)	On Cap (pF)	I_S (µA)	V_S (V)	Package
ISL43110	Single NO	11	37	21	220	15	40	0.05	+2.4 to +12	5 Ld SOT-23, 8 Ld SOIC
ISL84514	Single NO	13	47	28	220	14	30	2 (Max)	+2.4 to +12	5 Ld SOT, 8 Ld SOIC
ISL43144	Quad NO	18	52	40	330	10	34	0.01	+2 to +12, ±2 to ±6	16 Ld QFN, 16 Ld TSSOP
ISL8392	Quad NO	20	60	30	330	12	34	0.01	+2 to +12, ±2 to ±6	16 Ld SOIC
ISL43210	Single 2x1	19	25	17	500	8	28	0.05	+2.7 to +12	6 Ld SOT-23
ISL43231	Triple 2x1	81	32	18	250	3	14	0.1	+2 to +12, ±2 to ±6	20 Ld QFN
ISL84053	Triple 2x1	125	50	40	250	3	14	0.1	+2 to +12, ±2 to ±6	16 Ld QSOP, 16 Ld SOIC
ISL43240	Quad 2x1	30	52	40	330	10	30	0.01	+2 to +12, ±2 to ±6	20 Ld QFN, 20 Ld SSOP
ISL8394	Quad 2x1	25	50	30	330	12	39	0.01	+2 to +12, ±2 to ±6	20 Ld SOIC
ISL43640	Single 4 x1	115	25	24	350	4	20	0.0001	+2 to +12	10 Ld MSOP, 16 Ld QFN
ISL43840	Dual 4x1	81	32	18	250	3	18	0.1	+2 to +12, ±2 to ±6	20 Ld QFN
ISL43841	Dual 4x1	81	32	18	250	3	18	0.1	+2 to +12, ±2 to ±6	20 Ld QFN
ISL43741	Diff 4x1	81	32	18	280	3	18	0.1	+2 to +12, ±2 to ±6	20 Ld QFN
ISL43681	Single 8x1	81	32	18	250	3	26	0.1	+2 to +12, ±2 to ±6	20 Ld QFN

Eliminate Extra Voltage Supply with Integrated Triple +3.3V Video Buffer

The ISL59830 triple video buffer delivers DC-accurate coupling of video onto a 75Ω double-terminated line, and 300MHz of -3dB bandwidth performance.

Available in Pb-Free Package

ISL59830 Functional Block Diagram



Key Features:

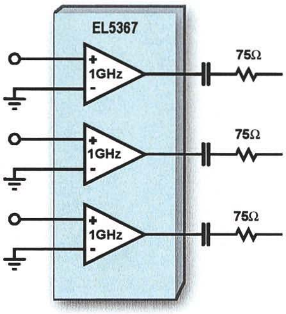
- Triple single-supply buffer
- Operates from single +3.3V supply
- Eliminates need for DC blocking capacitors
- Fixed gain of 2 output buffer
- Output 3-statable
- Enable/disable functions
- 50MHz 0.1dB bandwidth
- 300MHz -3dB bandwidth

Video Amplifiers - Rail-to-Rail

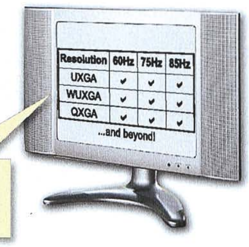
Device	# of Amps	BW @ -3dB (MHz)	SR (V/µs)	V_S (V)	V_N (nV√Hz)	Rail-to-Rail	Gain A_V (min) (V)	I_S (mA)	I_{BIAS} (mA)	I_{OUT} (mA)	V_{OUT} (V)	V_{OS} (max)(mV)	Package
EL8100	1	200	200	3.3 to 5	20	Out	1	2	1.5	80	0.1 to 4.9	6	6 Ld SOT-23, 8 Ld SOIC, 8 Ld SOT-23
EL8101	1	200	200	3.3 to 5	20	Out	1	2	1.5	80	0.1 to 4.9	6	5 Ld SOT-23
EL8102	1	500	600	3.3 to 5	12	Out	1	5.6	6	150	0.1 to 4.9	8	6 Ld SOT-23, 8 Ld SOIC
EL8103	1	500	600	3.3 to 5	12	Out	1	5.6	6	150	0.1 to 4.9	8	5 Ld SOT-23
EL8200	2	200	200	3.3 to 5	20	Out	1	2	1.5	65	0.1 to 4.9	6	10 Ld MSOP
EL8201	2	200	200	3.3 to 5	20	Out	1	2	1.5	80	0.1 to 4.9	6	8 Ld SOIC
EL8202	2	500	600	3.3 to 5	12	Out	1	5.6	6	65	0.1 to 4.9	8	10 Ld MSOP
EL8203	2	500	600	3.3 to 5	12	Out	1	5.6	6	150	0.1 to 4.9	8	8 Ld MSOP, 8 Ld SOIC
EL8300	3	200	200	3.3 to 5	20	Out	1	2	1.5	80	0.1 to 4.9	6	16 Ld QSOP, 16 Ld SOIC
EL8302	3	500	600	3.3 to 5	15	Out	1	6	6	150	0.1 to 4.9	8	16 Ld QSOP, 16 Ld SOIC
EL8401	4	200	200	3.3 to 5	20	Out	1	2	1.5	80	0.1 to 4.9	8	14 Ld SOIC, 16 Ld QSOP
EL8403	4	500	600	3.3 to 5	12	Out	1	5.6	6	65	0.1 to 4.9	8	14 Ld SOIC, 16 Ld QSOP
ISL59830	3	200	500	3.0 to 3.6	20	Y	2	50	N/A	50/-18	-1.8 to 3.3	25	16 Ld QSOP

World's Fastest Triple Current Feedback Amp

Drive QUXGA with one device



Named **"Best Video Op Amp"** in 2004 by analogZONE.



Support all existing resolutions with slew rates ~5000V/μs.

Video Amplifiers - High Speed (>50MHz)

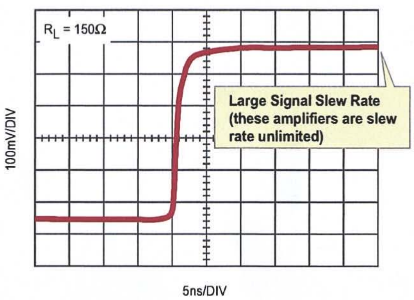
	Device	# of Amps	BW @ -3dB (MHz)	Slew Rate (V/μs)	V_S (min) (V)	V_S (max) (V)	V_N (nV/√Hz)	Gain A_V (min) (V)	I_S (per amp) (mA)	I_{OUT} (mA)	V_{OUT} (V)	V_{OS} (max) (mV)
Current Feedback	EL5160, EL5161	1	200	1700	±2.5	±5.5	4	1	0.75	70	±3.4	5
	EL5260, EL5261	2	200	2000	±2.25	±6.6	4	1	0.75	70	±3.4	5
	EL5360	3	200	1700	±2.25	±6.3	4	1	0.75	70	±3.4	5
	EL5162, EL5163	1	500	4000	±2.5	±5.5	3	1	1.5	100	±3.6	5
	EL5262, EL5263	2	500	2500	±2.25	±6.6	3	1	1.5	100	±3.6	5
	EL5362	3	500	2500	±2.25	±6.3	3	1	1.5	100	±3.6	5
	EL5462	4	500	4000	±2.5	±5.5	3	1	1.5	100	±3.75	1.5
	EL5164, EL5165	1	600	4700	±2.5	±5.5	2.1	1	3.5	140	±3.8	3.5
	EL5364	3	600	4200	±2.25	±6.3	2	1	3.5	140	±3.8	5
	EL5191	1	1000	2800	±2.25	±5.5	3.8	1	9	120	±3.7	15
	EL5367	3	1000	5000	±2.25	±5.5	1.7	1	8.5	160	±3.8	5
	EL5166	1	1400	6000	±2.5	±5.5	1.7	1	8.5	160	±3.8	5
Voltage Feedback	EL5170	1	100	1100	±2.25	±6.0	28	2 (Fixed)	7	80	±3.3	25
	EL5370	3	100	1200	±2.25	±6.0	28	2 (Fixed)	7	85	±3.8	25
	EL5100, EL5101	1	200	2200	±2.25	±6.6	10	1	2.5	100	±3.4	4
	EL5300	3	200	2200	±2.25	±6.6	10	1	2.5	100	±3.4	4
	EL5371	3	250	700	±2.25	±6.0	26	1	7	70	±3.7	25
	EL5372	3	250	800	±2.25	±6.6	26	1	5	95	±3.6	25
	EL5106	1	350	4500	±2.25	±6.6	12	±1, 2 (Fixed)	1.5	125	±3.6	10
	EL5306	3	350	4500	±2.25	±6.6	12	±1, 2 (Fixed)	1.5	125	±3.6	10
	EL5102, EL5103	1	400	2200	±2.25	±6.6	6	1	5.2	150	±3.7	5
	EL5202, EL5203	2	400	2200	±2.5	±6.6	6	1	5.2	150	±3.9	5
	EL5302	3	400	2200	±2.25	±6.6	6	1	5.2	150	±3.7	5
	EL5173	1	450	900	±2.25	±6.0	25	2 (Fixed)	12	55	±3.6	30
	EL5108	1	450	4500	±2.25	±6.6	8	±1, 2 (Fixed)	3.5	135	±3.8	5
	EL5373	3	450	1100	±2.25	±6.0	25	2 (Fixed)	12	55	±3.6	30
	EL5308	3	450	4500	±2.25	±6.6	10	±1, 2 (Fixed)	3.5	135	±3.8	5
	EL5374	3	550	850	±2.25	±6.0	21	1	12	60	±3.8	25
	EL5375	3	550	900	±2.25	±6.6	21	1	10	60	±3.8	16
	EL5104, EL5105	1	700	3000	±2.25	±6.6	10	1	9.5	160	±3.8	10
	EL5204, EL5205	2	700	3000	±2.5	±5	10	1	9.5	160	±3.8	10
	EL5304	3	700	3000	±2.25	±6.6	10	1	9.5	160	±3.8	10

World's Highest Slew Rate Voltage Feedback Amplifiers

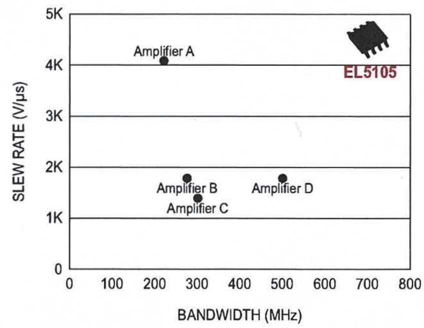
EL5104 and EL5105 provide unmatched AC performance in a voltage feedback architecture, use in place or any current feedback amplifier

Available in Pb-Free Package

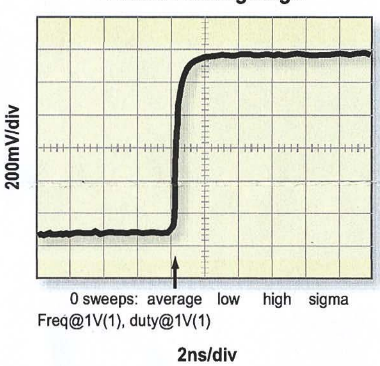
EL5105 Pulse Response



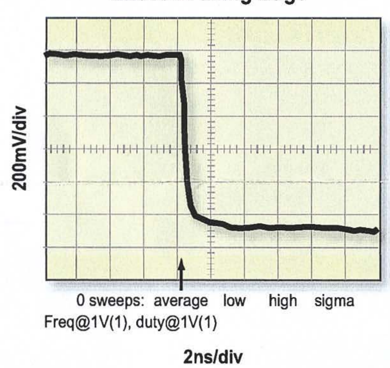
EL5105 vs Closest Competition



EL5104 Rising Edge



EL5104 Falling Edge



Key Features:

- Specified for 5V or ±5V applications
- Power-down to 17µA
- -3dB bandwidth: 700MHz
- ±0.1dB bandwidth: 45MHz
- Low supply current: 9.5mA
- Slew rate: 7000V/µs
- Low offset voltage: 10mV max
- Output current: 160mA
- A_{VOL} = 1400
- Diff gain/phase: 0.01%/0.02°

Device	# of Amps	BW @ -3dB (MHz)	Slew Rate (V/µs)	V_S (min) (V)	V_S (max) (V)	V_N (nV/√Hz)	Gain A_V (min) (V)	I_S (per amp) (mA)	I_{OUT} (mA)	V_{OUT} (V)	V_{OS} (max) (mV)
EL5100	1	300	2200	±2.25	±6.6	10	1	2.6	100	±3.4	5
EL5101	1	300	2200	±2.25	±6.6	10	1	2.6	100	±3.4	5
EL5102	1	450	3500	±2.25	±6.6	13	1	5.3	140	±3.6	5
EL5103	1	450	3500	±2.25	±6.6	13	1	5.3	140	±3.6	5
EL5104	1	700	4500	±2.25	±6.6	14	1	9.5	160	±3.8	5
EL5105	1	700	4500	±2.25	±6.6	14	1	9.5	160	±3.8	5
EL5202	2	40	3500	±2.5	±6.6	13	1	5.3	140	±3.6	5
EL5203	2	400	3500	±2.5	±6.6	13	1	5.3	140	±3.6	5
EL5204	2	700	4500	±2.5	±5	14	1	9.5	160	±3.8	5
EL5205	2	700	4500	±2.5	±5	14	1	9.5	160	±3.8	5
EL5300	3	200	2200	±2.25	±6.6	10	1	2.6	120	±3.4	5
EL5302	3	400	3500	±2.25	±6.6	13	1	5.3	140	±3.6	5
EL5304	3	700	4500	±2.25	±6.6	14	1	9.5	160	±3.8	5

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PCI Express and USB 2.0 improve performance of PC-based measurements

ADVANCES IN PC AND SILICON TECHNOLOGIES ALLOW LOW-COST, PC-BASED PLUG-IN DEVICES TO ACCURATELY AND QUICKLY PERFORM MEASUREMENTS AND CONTROL.

As PC technology has evolved, the ability to use standard desktop and portable computers for sophisticated test, control, and design applications has improved dramatically. Economies of scale have made it more cost-effective to use the gigahertz-speed processing and gigabytes of memory on standard computers than for vendors to install processors and memory in measurement instruments. Meanwhile, test-and-control vendors have repurposed commercially available silicon technologies. For example, ADCs and DACs for electronic devices, such as cellular phones and DVD players, now also provide speed and accuracy for PC-based data-acquisition devices. These high-production commercial components are available at fractions of the cost and in much faster design cycles than it would take for instrumentation vendors to design their own components. With these advances in PC and silicon technologies, low-cost, PC-based plug-in devices can now perform measurements and control with accuracy and processing speed that traditional instruments lack.

As acquisition rates increase, a common bottleneck for these virtual instruments has been the ability to quickly and easily transfer data from the measurement device into PC memory. Traditional bus technologies, such as GPIB and RS232, often require instrumentation vendors to install local memory on the instrument to temporarily store data that cannot move to the PC fast enough because of bus-bandwidth limitations. As the PC industry over the past decade standardized the PCI bus, plug-in devices for this bus realized a 77-times increase in data bandwidth versus GPIB, and, in many cases, this increase reduced the requirement for deep onboard memory. Meanwhile, cabled-bus technologies, such as USB, became popular for test-and-measurement applications because of their portability and ease of use. As virtual instruments acquire more data at faster rates by using the latest ADC and DAC technologies, systems using PCI and USB have again encountered the bus itself as the limiting factor in efficiently transferring data to PC memory. To address this increasing hunger for bandwidth, new technologies, including PCI Express and high-speed USB 2.0, are enabling designers to stream huge amounts of data from devices to the PC, ensuring backward compatibility, and improving ease of use.

PCI EXPRESS HAS ARRIVED

PC and peripheral vendors, including Intel, jointly developed PCI Express and last year began shipping it in standard desktop PCs. Most desktop machines from the leading suppliers include at least one PCI Express slot. PCI Express maintains software compatibility with traditional PCI but replaces the physical bus with a 2.5-Gbps serial bus. Data travels in packets through "lanes," pairs of transmitting and receiving signals that enable 250-Mbyte/sec bandwidth per direction per lane. Designers can

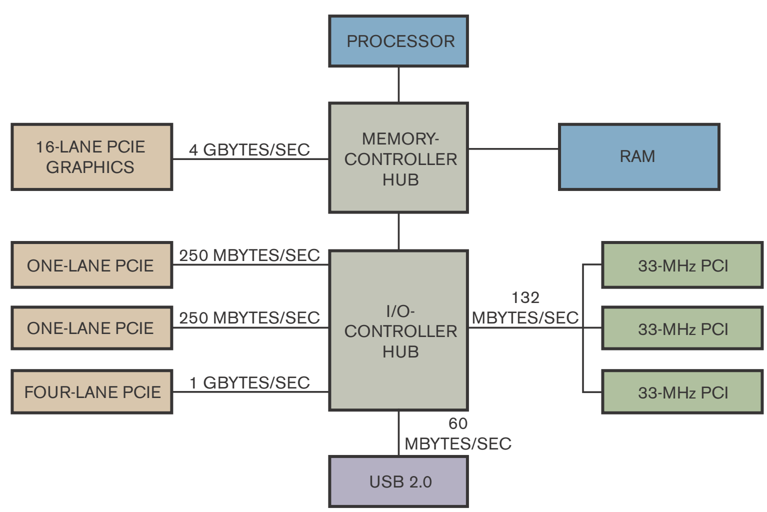

Figure 1 Each PCI Express slot has dedicated bandwidth to memory, unlike PCI, which shares bandwidth.

group multiple lanes of two, four, eight, 12, 16, and 32 to increase bandwidth to the slot. And, unlike PCI, which divides bandwidth between all devices on the bus, PCI Express provides dedicated bandwidth to each slot in the system.

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BANDWIDTH AND LATENCY

Applications such as data acquisition and waveform generation require guaranteed bandwidth and deterministic latency—the time for a system to send and another system to receive a signal, such as a configure or start command. Sufficient bandwidth ensures that data can transfer to memory fast enough without becoming lost or overwritten. Long latency is characteristic of buses such as Ethernet and is a primary reason that PC-based test-system vendors have not widely adopted this bus. The original PCI specification did not address these issues because high-speed-data-streaming applications on the PC were not prevalent at the time. As a result, data-acquisition devices that adopted the bus required onboard memory for data buffering to handle the varying bandwidths available during data transfers (see **sidebar** "Data-acquisition devices emerge"). Today, isochronous data transfers such as uncompressed streaming audio and video require the I/O subsystem of the PC to provide guaranteed bandwidth and deterministic latency to prevent data glitches. To address these needs, PCI Express incorporates an isochronous data-transfer mode, allowing a device to reserve a defined amount of bandwidth with deterministic latency. Data-acquisition applications also benefit from this feature, because PCI Express devices require less memory than traditional PCI for data-buffering purposes (**Figure 1**).

PCI Express dramatically improves data bandwidth. The initial signaling frequency of 2.5 Gbps with a 16-lane slot provides as much as 30 times (60 times in two directions) the usable bandwidth of 32-bit, 33-MHz PCI, and, with advances in silicon technology, this signaling frequency should increase toward 10 Gbps—the practical limit for signals in copper. Because of the lane topology of PCI Express, data-acquisition-system vendors can implement a PCI Express connector with the number of lanes suitable to the requirements of the device. They can plug devices with smaller connectors into larger host connectors on the motherboard, improving hardware compatibility and flexibility (**Figure 2**).

SOFTWARE COMPATIBILITY IS PARAMOUNT

The PCI Express specification also ensures software compatibility. The configuration space and programmability of PCI Express devices remain unchanged from the traditional PCI

DATA-ACQUISITION DEVICES EMERGE

National Instruments recently released the industry's first PCI Express data-acquisition devices (Figure A). The new NI PCIe-6251 and 6259 devices combine the high-performance PCI Express bus with the technological advancements of National Instruments M Series devices to offer engineers and scientists fast analog and digital I/O with the dedicated per-slot bandwidth of PCI Express. The new devices feature as many as 32 analog channels with 16-bit, 1.25M-sample/sec speed, and 10-MHz digital I/O on as many as 32 lines. They use a one-lane PCI Express connector; one lane is the most common PCI Express lane width on currently shipping desktop PCs. These two new data-acquisition devices complement the PCI Express image-acquisition and GPIB devices that the company released in 2004.

As with other NI M Series DAQ devices, the new NI PCIe-6251 and NI PCIe-6259 feature the NI-STC 2 system controller, the NI-PGIA 2 amplifier, and NI-MCal calibration technology for increased performance, accuracy, and I/O. The devices are part of the high-speed M Series family, offering as many as four analog-output channels at 16 bits at 2.8 MHz and 32 high-speed digital lines at 10 MHz. The devices also include 48 digital-I/O lines and two 32-bit counter/timers. The devices come with measurement software, including NI-DAQmx driver software and VI Logger Lite data-logging software. Because of the software compatibility that the PCI Express standard provides, all examples and applications for PCI-based M Series devices are compatible with their new PCI Express counterparts.

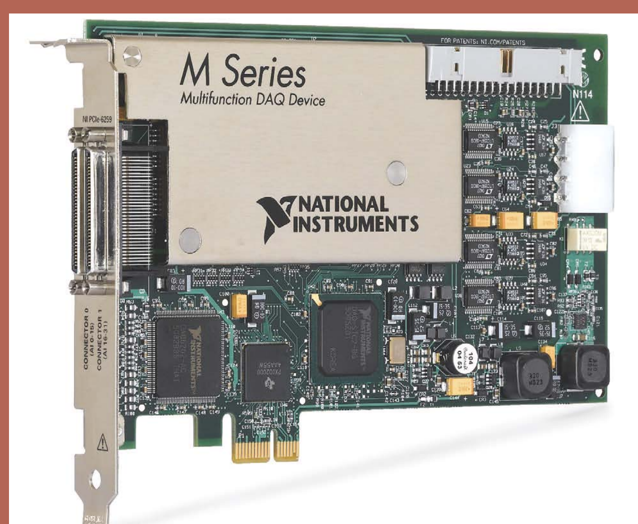


Figure A The NI PCIe devices offer fast analog and digital I/O with the dedicated per-slot bandwidth of PCI Express.

methodology. All operating systems can boot without modification on a PCI Express architecture. At boot time, the operating system can discover all of the PCI Express devices present and then allocate system resources, such as memory, I/O space, and interrupts to create an optimal system environment. And, because the PCI Express physical layer is transparent to application software, programs written for PCI devices can run unchanged on PCI Express devices that have the same functions. This backward compatibility of PCI Express software with traditional PCI is critical in preserving the software investments of both vendors and users.

Similar to the improvements PCI Express offers plug-in devices, high-speed USB 2.0 has improvements in bandwidth and signal latency for externally cabled data-acquisition devices. USB has become the de facto standard for cabling peripheral devices to the PC, and data-acquisition devices are no exception. The plug-and-play and hot-pluggable features of the bus make it easy to use, enabling a host PC to automatically detect and configure a connected device. Users can dynamically load and unload drivers without powering down the device or PC during installation. USB 2.0 also provides power on the same cable that carries the data signal, often simplifying connectivity and portability by eliminating dedicated ac power cables.

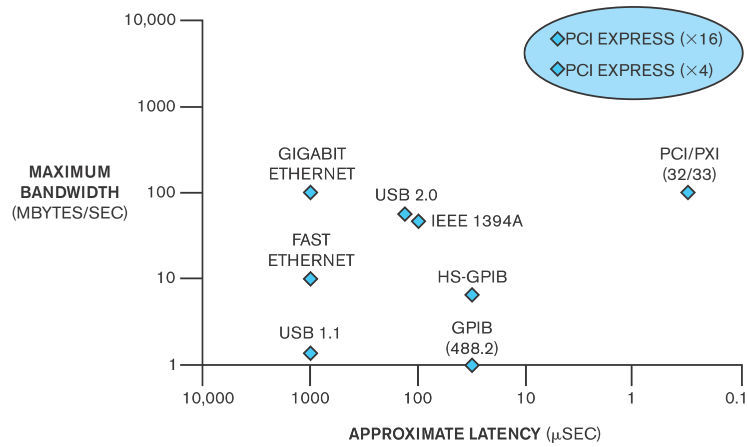


Figure 2 PCI Express dramatically improves data bandwidth.

The USB 2.0 specification made significant improvements in both bandwidth and latency versus USB 1.1. The 1.5-Mbyte/sec rate that USB 1.1 provided quickly became a limiting factor for large data transfers, such as those for high-speed data acquisition. High-speed USB 2.0 improved that rate by 40 times, enabling bandwidths as large as 60 Mbytes/sec. Like PCI Express, USB 2.0 provides isochronous transfers but also adds three data-transfer modes that the manufacturer can enable. For example, the bulk-transfer mode provides data-reception confirmations to ensure error-free transfer for applications such as data acquisition in which data integrity is paramount.

AS PC-BUS TECHNOLOGIES, SUCH AS PCI EXPRESS AND USB 2.0, CONTINUE TO IMPROVE DATA BANDWIDTH, PERFORMANCE, AND EASE OF USE, THE BENEFITS OF USING PC-BASED DEVICES FOR MEASUREMENTS AND CONTROL BECOME EVEN MORE DRAMATIC.

The release of the USB 2.0 standard created low-speed, 1.5-Mbps; full-speed, 12-Mbps; and high-speed, 480-Mbps classes of USB devices. USB 2.0 is both forward- and backward-compatible with USB 1.1, and low-speed, full-speed, and high-speed devices can all coexist on a single USB port. In addition to bandwidth improvements, USB 2.0 also introduced ways to improve the efficiency of data transfers. Data frames—the time segments for packet transfers—decreased from 1 msec to eight 125-μsec frames, and the number of data bytes transferred per frame significantly increased. Because large data packets can consume large amounts of bandwidth, new handshaking commands ensure that the host is ready and able to receive the entire queued data packet. USB 2.0 also introduced split transactions, which prevent full- and low-speed devices from slowing the bus. With split transactions, the host can communicate with high-speed devices on the bus without waiting for slower devices to return communication.

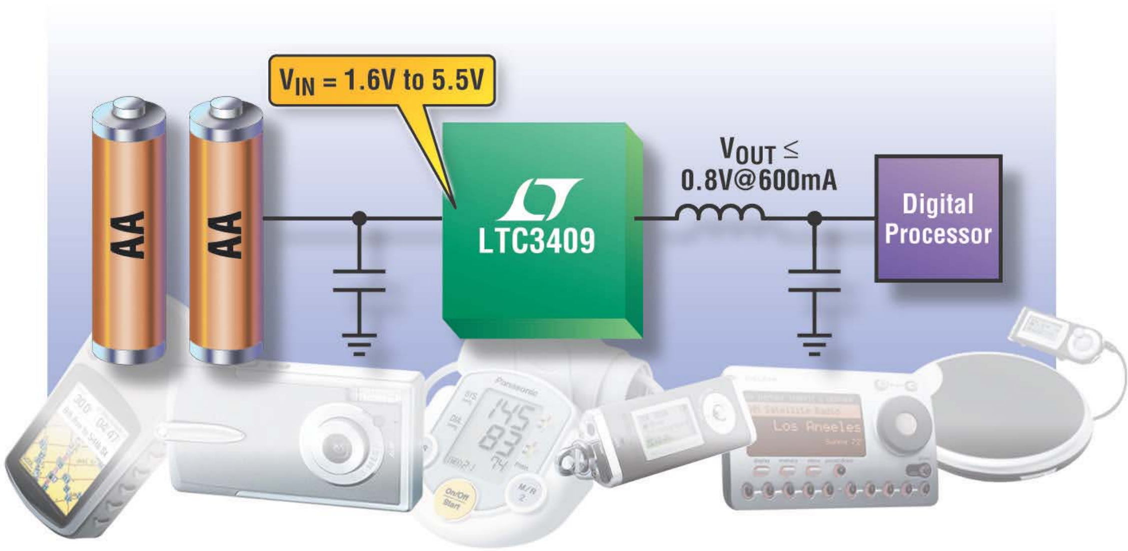
WHAT'S AHEAD?

As PC-bus technologies, such as PCI Express and USB 2.0, continue to improve data bandwidth, performance, and ease of use, the benefits of using PC-based devices for measurements and control become even more dramatic. By virtue of being based on computer technology, virtual instruments will always improve as new communication, processing, and memory technologies come to market. As PCI Express and USB 2.0 continue in their adoption cycles, hybrid systems for several years will use these new technologies in addition to traditional PCI and USB 1.1 buses and devices. The software compatibilities of the new technologies as well as the physical compatibility between USB 1.1 and USB 2.0 will bridge these devices with their predecessors. But the benefits of these two new technologies are clear, and, as PC-based test-and-control systems continue to push bandwidth requirements, PCI Express and USB 2.0 will enable faster data transfers to PCs, which can fully use the ever-increasing processor speeds and memory depths. USB 2.0 has spurred a whirlwind of new, easy-to-use data-acquisition devices, and, with the release of PCI Express, the next generation of plug-in data-acquisition devices adopting the new bus standard is sure to follow. EDN

AUTHOR'S BIOGRAPHY

Brian Betts is data-acquisition-systems group manager at National Instruments. He has a bachelor's degree in mechanical engineering from Texas A&M University (College Station, TX). You can reach him at brian.betts@ni.com.

2 AA Buck Regulator



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- Very Low Quiescent Current: Only 60µA in Burst Mode® Operation
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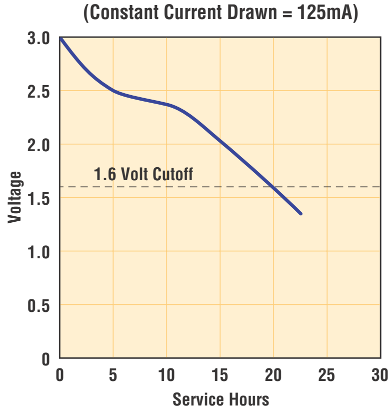
- 8-Lead 3mm x 3mm x 0.75mm DFN package

Discharge Profile of 2 AA Cells
(Constant Current Drawn = 125mA)



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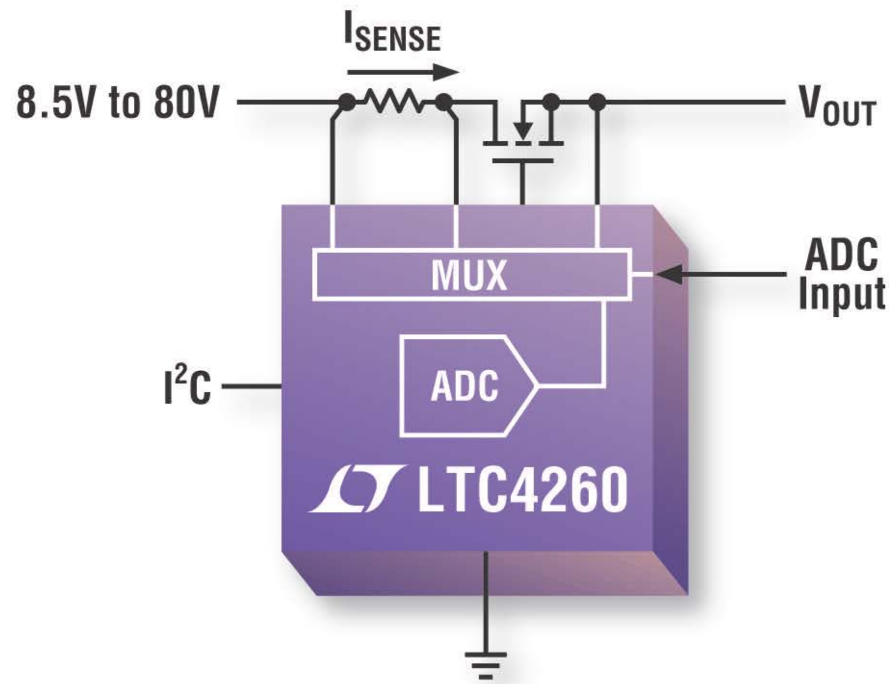
Hot Swap with ADC



High Voltage Controller with Integrated ADC Measures Board Current, Voltage & Fault Status

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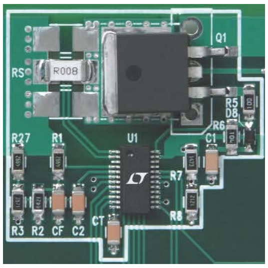
- Input Overvoltage/Undervoltage Protection
- Alerts Host After Faults
- LTC4260: $6.50 each in 1k Qty

Quick Evaluation System



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LINEAR TECHNOLOGY

Keyboard links to microcomputer through one-wire interface

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DIs Inside

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A previous Design Idea described a single-wire-plus-ground-return, keypad-to-microcontroller interface in which a single pulse represents each keystroke (**Reference 1**). The pulse's width is proportional to the key's numerical value, and the microcontroller identifies the pressed key by measuring the pulse width. Component tolerances and the accuracy of the microcontroller's internal oscillator limit the original design to keypads with 16 or fewer keys—that is, four rows by four columns or smaller cross-point-key matrix. This Design Idea illustrates how a relatively simple modification applies the method to much larger keypads. (The following description omits a few details from the original Design Idea, which you can find online at www.edn.com/article/CA512131.)

You can divide a large keypad or keyboard into sections of 12 keys each (**Figure 1**). Each section connects to a separate comparator circuit, which detects a keystroke and generates a trigger pulse using the monostable circuit of IC_4, and you can add more sections in the same manner. Diodes D_1, D_2, and D_3 couple and isolate the comparators' outputs to Pin 2 of IC_4. Each keypad section connects the same selection of timing-resistor values to the monostable. Therefore, each keypad section's output pulse widths occupy the same range: 110 to 1320 μsec.

For the microcontroller to identify an active keypad section, the circuit generates a single, double, or triple pulse, depending on whether the pressed key

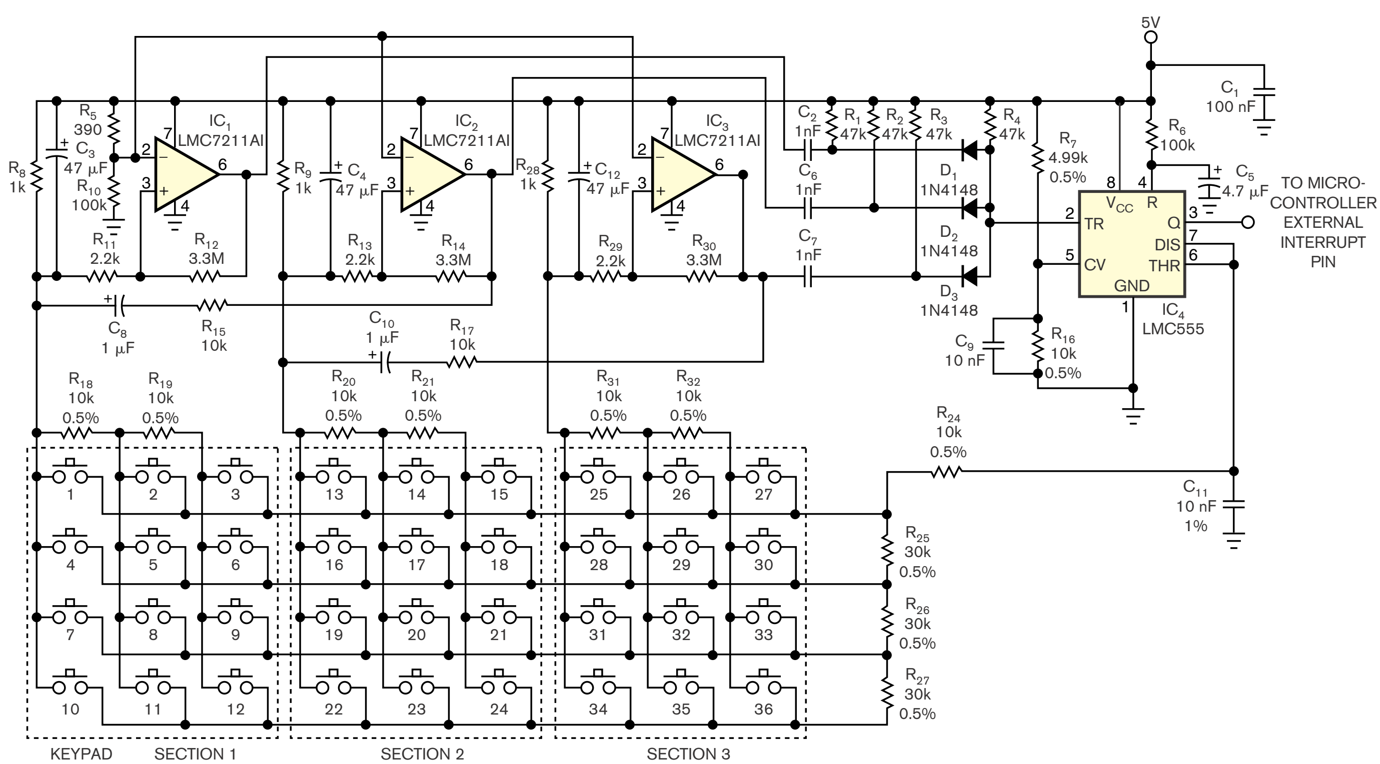

Figure 1 A keyboard encoder uses multiple variable-width pulses to communicate keys' addresses to a microcontroller using a single-wire interface.

resides in section 1, 2, or 3, respectively. The microcontroller identifies the pressed key by measuring the width of the first pulse and identifies the keypad section by counting the number of pulses. Implementing the multiple-pulse-encoding scheme requires no additional active components. Pressing a key in Section 1 generates a single pulse. Pressing a key in Section 2 causes comparator IC_2's output to go low and triggers IC_4 to generate the first pulse. At the same time, R_{15} and C_8 apply IC_2's output transition to comparator IC_1's input. As IC_2's output, Pin 6, goes low, C_3 starts to charge, and, after a delay of about 2 msec, IC_1 triggers IC_4 to generate the required second pulse. Because the time-constant product of $R_{15}\times C_8$ is much longer than 2 msec, C_8 does not charge significantly during the 2-msec interval. However, C_8 does charge to a full 5V during the interval in which the key is pressed, which allows comparator IC_1 to recover to its steady state.

In a three-section keypad, pressing a key in the third section activates comparator IC_3 which in turn triggers IC_4 to produce the first pulse. After feedback through R_{17} and C_{10} produces a 2-msec delay, IC_2 triggers IC_4 to produce a second pulse. After yet another 2-msec delay, IC_1 triggers IC_4 to produce the third and final pulse. Although somewhat arbitrary, a 2-msec delay provides sufficient margin over the maximum key-pressed pulse width of 1.32 msec. The interrupt routine provides additional timing margin by allowing as much as 3 msec between pulses.

Listing 1, available in the online version of this Design Idea at www.edn.com/050929di1, represents a modified version of the interrupt routine in **Reference 1** and supports the circuit in **Figure 1** for any number of keypad sections. For a three-section-keyboard implementation, the routine returns a key number from 1 to 36. EDN

REFERENCE

1. Schleicher, Israel, "Single-wire keypad interface frees microcontroller-I/O pins," *EDN*, March 31, 2005, pg 75, www.edn.com/article/CA512131.

Added components improve switching-regulator stability

Wayne Rewinkel, National Semiconductor, Schaumburg, IL

This Design Idea shows how adding one or two passive parts can reduce a hysteretic constant-on-time switched-mode voltage regulator's output voltage ripple and reduce its susceptibility to variations in external load capacitance and ESR (equivalent series resistance). The regulator operates much like a pure hysteretic switcher. The device's internal one-shot sets its pass transistor's on-time, making it less prone to frequency runaway but still susceptible to noise injected at the regulator's FB (feedback) pin. To switch cleanly with predictable frequency and duty cycle, the switcher requires application of approximately 50 to 100 mV of ripple voltage to the feedback pin. This Design Idea shows how four circuit implementations using National's LM5007 and LM5008 regulators satisfy the important feedback-ripple requirements by adjusting on-resistance and maintaining a nearly constant switching frequency as input voltage varies.

Figure 1 shows a basic buck regulator whose output capacitor, C_5, presents a high internal ESR, R_5. Note that the designer cannot access R_5 and V_{OUT2}. Inductor L_1's ripple current flows through R_5 and C_5 and produces a certain amount of ripple voltage at V_{OUT1}. Although common, this simple design presents two problems: First, feedback resistors R_4 and R_3 form a voltage divider that reduces the output ripple presented to IC_5's FB pin. Thus, 50 mV of ripple at the pin may correspond to excessive ripple voltage at V_{OUT1}. Adding a compensation capacitor, C_4, forces the output-ripple voltage to appear at the feedback pin. Second, a typical pc board may include many low-ESR ceramic bypass capacitors that attenuate ripple voltage to a level that destabilizes the circuit.

Suppose that you replace C_5 in **Figure 1** with a low-ESR capacitor and add R_5 as a discrete resistor. You can connect the external load to V_{OUT2} to reduce output-ripple voltage at the load

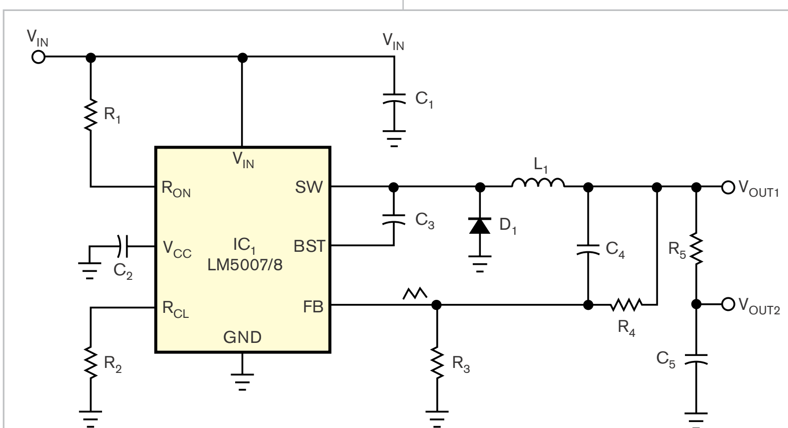

Figure 1 This basic switched-mode voltage regulator reduces its input voltage to a lower value.

and increase the circuit's immunity to added load capacitance. The regulator's feedback voltage derives from V_{OUT1}, and C_4 reduces output-ripple losses in the feedback divider, R_4 and R_3. Unfortunately, this frequently used design introduces new problems: As output current increases, V_{OUT2} falls below V_{OUT1} and degrades load-voltage regulation. Second, R_5 carries full load current and dissipates power, reducing overall efficiency. Using a large, high-wattage fractional-ohm resistor at R_5 increases product cost and regulator-package dimensions.

Figure 2 shows a rearranged buck-mode-switching regulator with two additional components. Assume that C_5's ESR is negligible and that R_6 is open. Now, R_5 remains inside the feedback loop, and C_4 couples voltage ripple from the inductor side of R_5 to feedback. This action stabilizes the regulator's operation and requires almost no output-ripple voltage, and R_5 introduces only a small reduction in efficiency. Taking dc feedback at the load preserves the circuit's excellent load regulation.

In another scenario, suppose that you replace R_5 with a short circuit and select values for R_6 and C_4 that provide the desired amount of ripple voltage at the feedback pin. This configuration produces almost no output-voltage ripple and eliminates R_5's power losses. Load regulation suffers because, as load current increases, inductor L_1's ESR introduces voltage droop at V_{OUT1} and forces the voltage at switching node SW slightly higher. However, designers can select L_1 for a low ESR that minimizes its effects on load regulation and can make R_6's resistance larger than that of R_4.

The following examples compare output ripple, circuit losses, and component count for the design scenarios. Assume that input voltage is 50V, output voltage is 5V, output current is 400 mA, switching frequency is 480 kHz, and desired minimum feedback ripple is 50 mV p-p. Select L_1 to operate at a ripple current of 200 mA. Solving for L_1, you obtain:

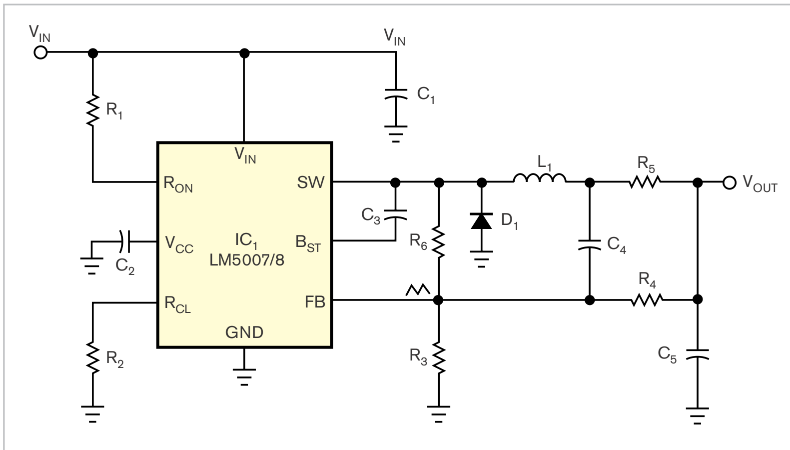

Figure 2 Adding two components, R_6 and C_4, helps reduce output-ripple voltage and improve output-voltage regulation.

$$L_1=\frac{(V_{IN}-V_{OUT})\times t_{ON}}{I_{RIPPLE}}=\frac{(50-5)\times t_{ON}}{0.2}.$$

$$t_{ON}=\frac{V_{OUT}}{V_{IN}\times f_S}=\frac{5}{50\times 480\ k\Omega}=0.21\ \mu SEC.$$

Substituting on-time into the above **equation** yields

$$L_1=\frac{45\times 0.21}{0.2}=47\ \mu H.$$

Select a Coilcraft DO1813P-473HC with ESR of 0.47Ω based on its small pc-board footprint. For C_5, choose a ceramic capacitor that's large enough to limit the ripple voltage on V_{OUT} to less than 10 mV p-p. Given the maximum ripple voltage and a known triangle-wave current drive, calculate a value for C_5:

$$C_5=\frac{I_{RIPPLE}}{(8\times V_{RIPPLE}\times f_S)}=\frac{0.2}{(8\times 0.010\times 480\ kHz)}=5.2\ \mu F.$$

For C_5, you can use TDK's 10-μF C3216X7R0J106 ceramic capacitor that presents an ESR of 3 mΩ or less. Because the internal reference voltage for the LM5007 or LM5008 is 2.5V, set feedback resistors R_3 and R_4 to 1 kΩ to divide the regulator's 5V output to 2.5V. Next, select values for R_5, C_4, and R_6 to compare results for each design. In the first scenario, to provide 100 mV of ripple at V_{OUT1} and 50-mV ripple at the feedback pin in the circuit of **Figure 1**, the design requires a value of 0.25Ω for R_5. Adding C_4 changes the value of R_5 to 0.125Ω to provide 50-mV ripple at V_{OUT1} and the feedback pin. You calculate a value for C_4 that passes the ripple current:

$$C_4=\frac{10}{(2\pi(R_4\|R_3)\times f_S}=\frac{10}{(2\times 3.14159\times 500\times 480\ k\Omega)}=6.6\ nF,$$

TABLE 1 CIRCUIT OPTIONS

Scenario	Figure	R_5 (Ω)	R_6 (Ω)	C_4 (nF)	V_{OUT}, R_6 (mV)	Voltage droop (mV)	Power dissipation (mW)	Issues
1	1	0.25	0	0	100	0	0	Load capacitance and stability
1	1	0.125	0	6.6	50	0	0	Load capacitance and stability
2	1	0.25	0	0	6	100	40	Voltage droop and power dissipation
2	1	0.125	0	6.6	6	50	20	Power dissipation
3	2	0.125	0	6.6	6	0	20	Power dissipation
4	2	0	30k	6.6	6	7	0	Voltage droop

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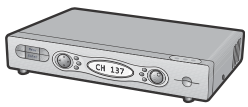

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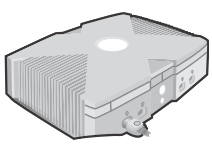

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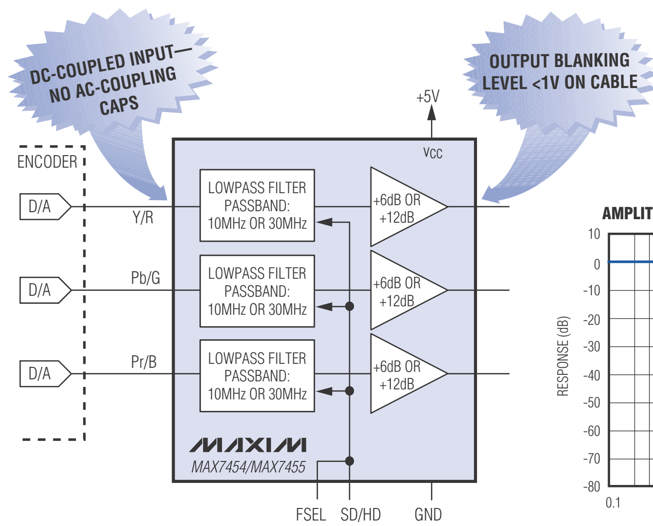

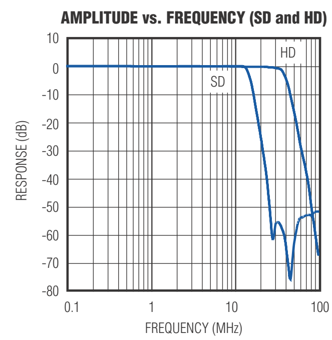

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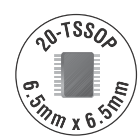
MAX7455	3	Yes	+4	20-TSSOP	2.75



†1000-up recommended resale. Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates. Not all packages are offered in 1k increments, and some may require minimum order quantities.

where $R_4 || R_3$ represents the value of the parallel combination of R_4 and R_3.

In the second scenario, V_{OUT2} droops to 100 mV at full load but exhibits only 6 mV of ripple without C_4 in the circuit. Losses in R_5 amount to 40 mW. Adding C_4 delivers 50 mV of ripple to the feedback pin and V_{OUT1}; setting R_5 to 0.125Ω reduces R_5's power loss to 20 mW. In the third scenario, R_6 is an open circuit, and the design in **Figure 2** requires an R_5 value of 0.125Ω to provide 50-mV ripple at FB. V_{OUT1} exhibits no voltage droop at full load current and has only 6 mV of ripple voltage. R_5's power loss is 20 mW.

In the fourth case, a short circuit replaces R_5, and the design in **Figure 2** requires a value for R_6 that increases the voltage across C_4 to provide 50 mV of ripple voltage at FB. Use the following **equations** to calculate the value:

$$R_6 = \frac{(V_{IN}-2.5)}{C_4 \times 50\text{ mV} \times V_{IN} \times ((f_S / V_{OUT}))} = 30\text{ k}\Omega.$$

$$R_{RIPPLE} = (V_{IN}-2.5)/(C_{RIPPLE} \times 50\text{ mV} \times V_{IN} \times f_S / V_{OUT}) = 30\text{ k}\Omega.$$

With R_6 in the circuit, V_{OUT} drops slightly because R_6 and R_4 effectively connect in parallel. To compensate, you can slightly increase R_4 so that the new value of R_4 in parallel with R_6 equals R_4's original value. Thus,

$$R_{4(NEW)} = \frac{R_{4(OLD)} \times R_6}{R_6 - R_{4(OLD)}} = \frac{1000 \times 30}{29} = 1.034\text{ k}\Omega.$$

In this instance, you may decide not to use the new value of R_4 because adding R_6 raises V_{OUT} by only 85 mV. Adding R_6 produces 6 mV of ripple at V_{OUT} and little or no loss in R_5, but load regulation will not be perfect.

Inductor L_1's ESR of 0.47Ω introduces a voltage drop of about 200 mV at full load, which increases the voltage at the junction of L_1 and R_6 and also reduces V_{OUT} to maintain 2.5V at FB. You can calculate the magnitude of the change by multiplying L_1's voltage drop of 200 mV by the ratio of R_4 to R_6:

$$V_{OUT(DROOP)} = \frac{200\text{ mV} \times R_4}{R_6} = \frac{0.2 \times 1}{30} = 0.0067\text{V}.$$

Note that output-voltage droop and power dissipation become more significant in designs that deliver higher output current or lower output voltage (**Table 1**). EDN

Electromechanical damping stabilizes analog-meter readings

Alexander Bell, Infosoft International Inc, Rego Park, NY

Before shipping moving-coil meters, manufacturers may short-circuit the meters' terminals with a length of wire, which provides effective electromagnetic damping and results in better immunity to external mechanical vibration and shocks that can occur during transportation. This Design Idea applies essentially the same principle to analog meters under normal operating conditions. Connecting a meter to a voltage source with low internal resistance applies electromagnetic damping and makes the meter's readings more stable. Increased immunity to external vibration and shock takes on importance in mobile- or portable-system applications and especially in automotive devices.

For example, suppose that your application requires measurement of a 0 to 10V power supply (**Figure 1**). You have available a typical electromechanical meter that presents a full-scale voltage rating, V_{FS}, of 50 mV and a full-scale current rating of 1 mA. To obtain the 10V full-scale voltage range, you add a series resistance, R_S. First, calculate the meter's internal resistance, R_{COIL}:

$$R_{COIL} = \frac{V_{FS}}{I_{FS}} = \frac{50\text{ mV}}{1\text{ mA}} = 50\Omega.$$

Next, calculate the multiplier resistor, R_S, as follows:

$$R_S = \frac{(V_{IN}-V_{FS})}{I_{FS}} = \frac{(10\text{V}-0.05\text{V})}{1\text{ mA}} = 9950\Omega.$$

The resistance of R_S typically great-

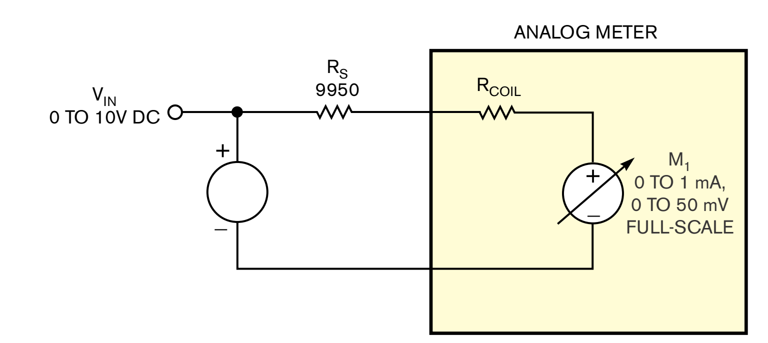


Figure 1 A typical analog moving-coil voltmeter employs a high-value series resistor, R_S, to establish the full-scale range but doesn't contribute to electromagnetic damping of the meter movement.

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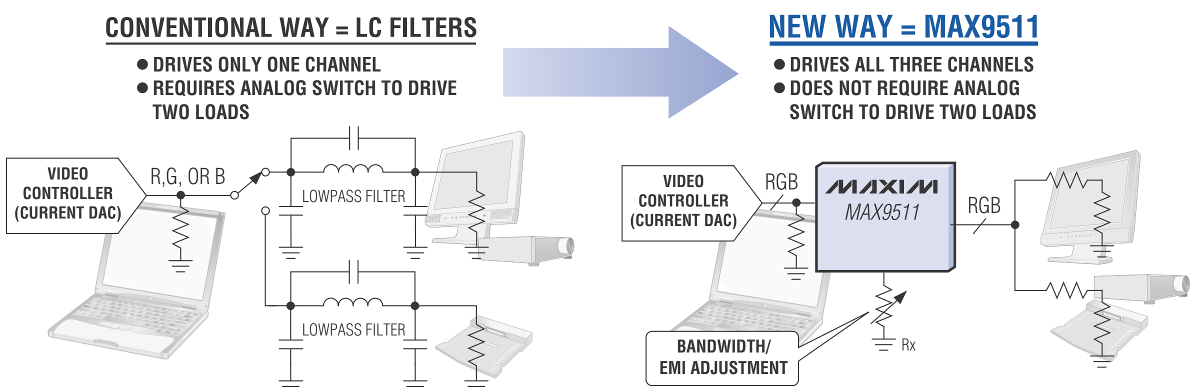

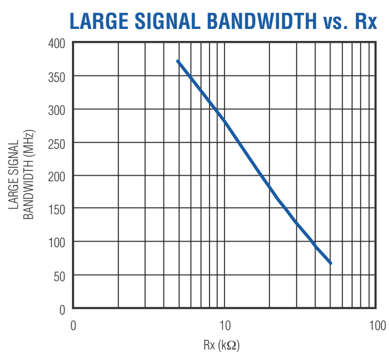

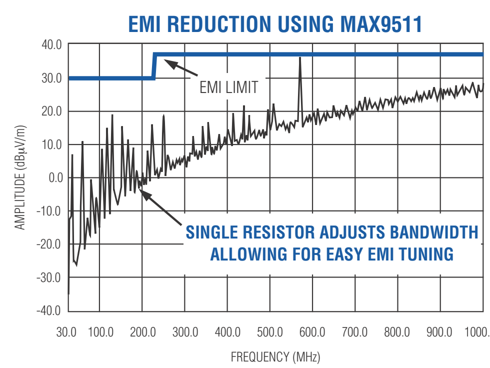

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ly exceeds that of R_{COIL} and therefore significantly reduces the electromagnetic damping action on the meter movement. Although you can improve damping by shunting the meter with a capacitor, this approach also increases the meter's settling time.

Figure 2 illustrates a better approach, in which a moving-coil meter connects to the output of an operational amplifier, IC_1, embedded in a deep negative-voltage-feedback loop. Because the op amp presents an extremely low equivalent output resistance, the meter's terminals are "virtually shorted," providing effective electromechanical damping that results in more stable readings and increased shock and vibration resistance. In **Figure 2**, the resistive voltage divider comprising R_1 and R_2 connected to the op amp's noninverting input determines the meter's full-scale reading. You can add R_F and C_F to form an optional highpass filter to further improve the meter's settling time. Transistors Q_1 and Q_2 are also optional and added as overvoltage protection. Note that, for normal operation, the transistors' forward base-emitter voltage, V_{BE}, should be several times larger than the meter's full-scale voltage, V_{FS}, which is typically 50 to 100 mV.

A rail-to-rail-capable, single-supply micropower op amp makes a good choice for this application. If the input voltage, V_{IN}, exceeds the op amp's minimum power-supply-voltage requirement, you can connect the op amp's V_{CC} pin directly to the input terminal, as the dashed line in **Figure 2** shows. In effect, the circuit combines the advantages of meter buffering and improved shock and vibration resistance with a traditional moving-coil meter's advantage of requiring no external power supply. You can choose from among many commercially available off-the-shelf, rail-to-rail output-micropower op amps that draw supply currents well below the full-scale current drain, I_{FS}, of typical moving-coil meters. For example, Maxim's MAX4289 requires as little as 1V and 9 μA of power, and the MAX4470 requires a minimum of 1.8V but only 750 nA of supply current.

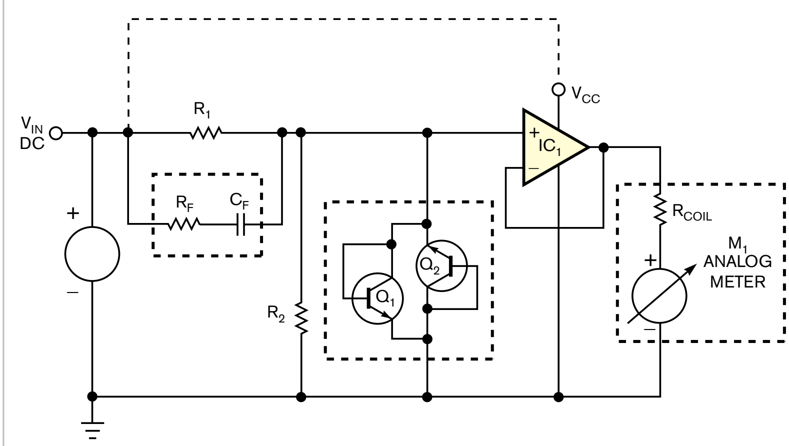

Figure 2 An operational amplifier's low output resistance provides electromechanical damping for a moving-coil meter for stable readings and enhanced resistance to mechanical shock and vibration. Connect V_{CC} to either an external power supply or the circuit's input terminal if V_{IN} exceeds IC_1's minimum power-supply-voltage rating.

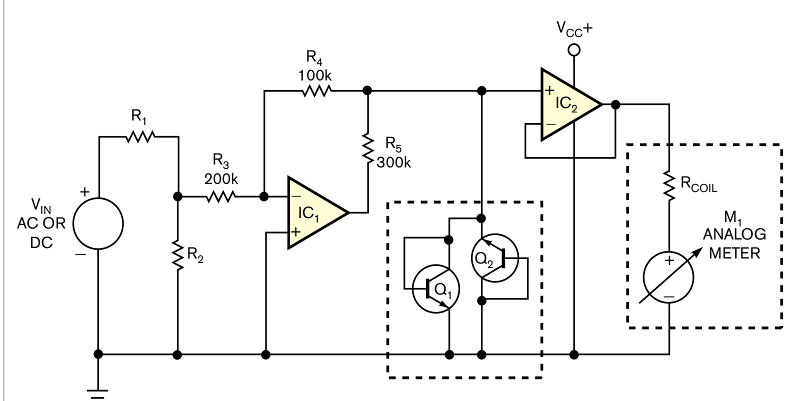

Figure 3 Based on rail-to-rail operational amplifier IC_1, this circuit's input stage forms a diodeless, precision full-wave rectifier and enables the circuit of Figure 2 to display ac- or dc-voltage measurements on a dc meter.

Although this Design Idea has so far related only to dc-voltage measurements, you can expand the circuit to include ac- and dc-voltage measurements (**Figure 3**). In this approach, you add a precision diodeless, full-wave-rectifier stage based on a single rail-to-rail operational amplifier and resistors R_3, R_4, and R_5 (**Reference 1**). Resistors R_1 and R_2 determine the full-scale reading. This circuit requires an external dc power supply to drive op amps IC_1 and IC_2; voltage-limiting transistors Q_1 and Q_2 are optional. EDN

REFERENCE

1. Bell, Alexander, "Simple Full-Wave Rectifier," *Electronic Design*, April 4, 1994, pg 78.

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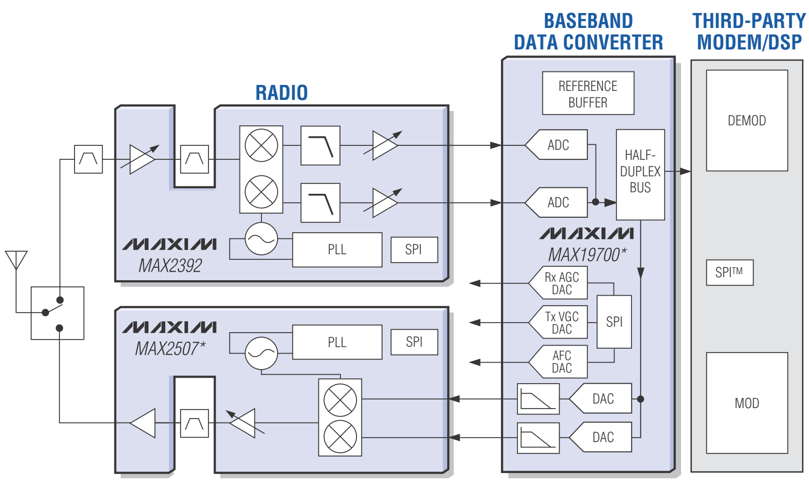

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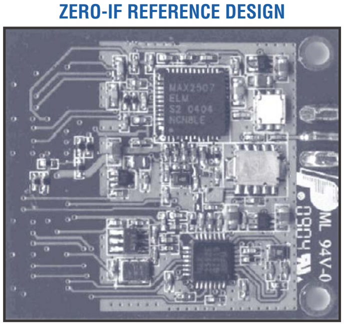

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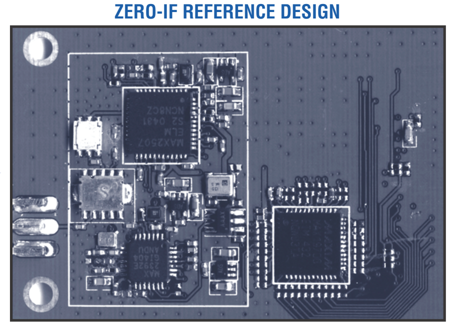

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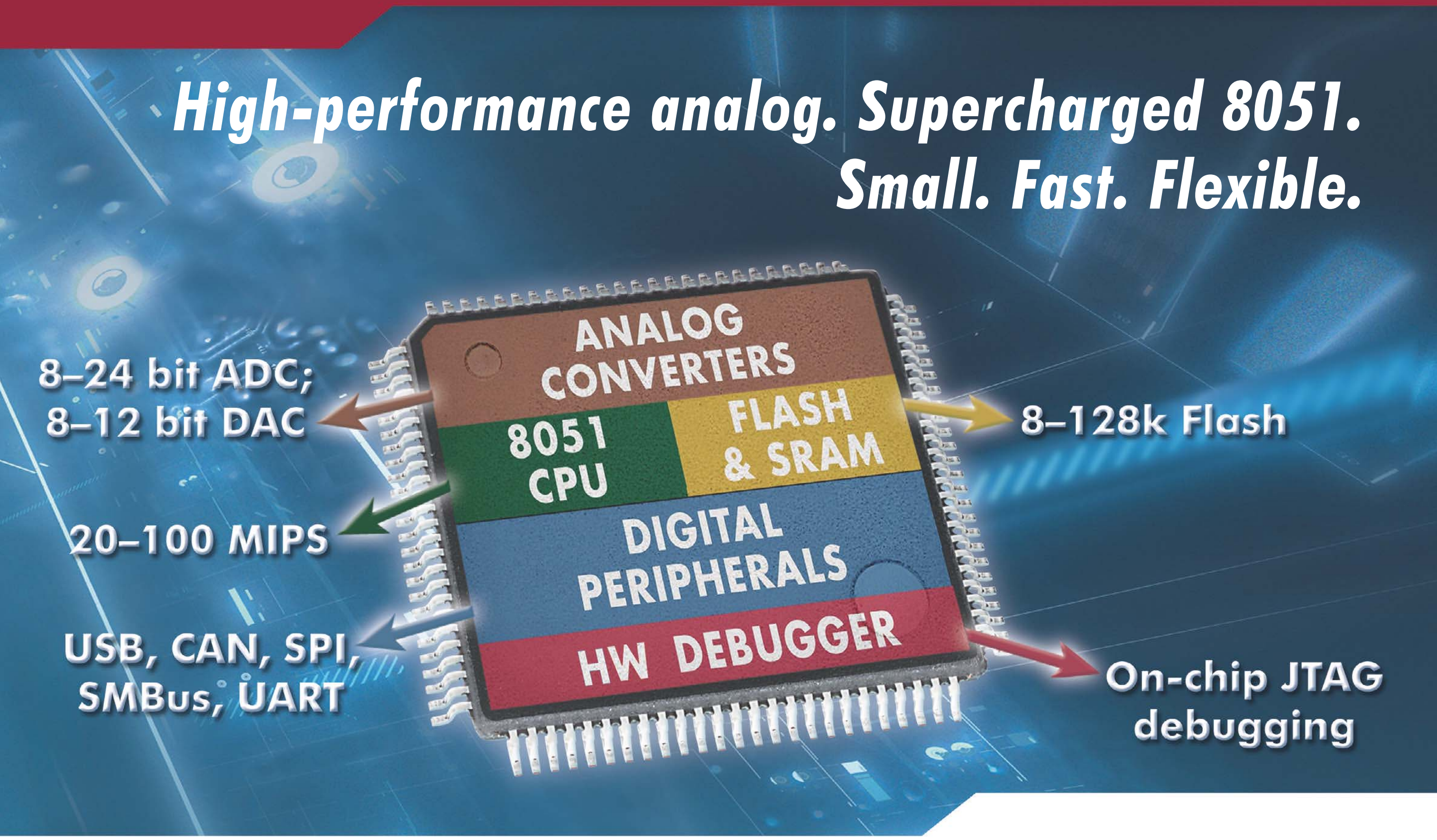

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DESIGN NOTES

Power Supply Tracker Can Also Margin Supplies – Design Note 372

Dan Eddleman

Power supply margining is a technique commonly used to test circuit boards in production. By adjusting power supply output voltages, electrical components are tested at the upper and lower supply voltage limits specified for a design. The LTC®2923 power supply tracking controller can be used to margin supplies in addition to its usual task of tracking multiple power supplies.

The LTC2923 uses the simple tracking cell shown in Figure 1 to control the ramp-up and ramp-down behavior of multiple supplies. This cell servos the TRACK input to 0.8V and mirrors the current supplied by that pin at the FB output pin. The FB pin connects to the feedback node of the slave power supply. Normally, a resistive divider connects the master signal to the TRACK pin. By selecting the appropriate resistor values, R_{TA} and R_{TB}, the relationship of the slave power supply is configured relative to the master signal.

The supply margining application uses an LTC2923 tracking cell to margin a supply high and low under the control of a three-state I/O pin.

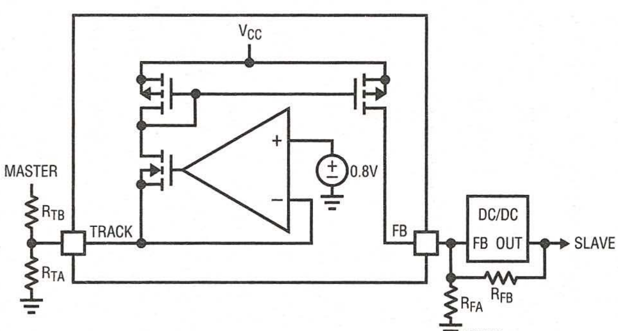

Figure 1. Simplified Tracking Cell

In the circuit shown in Figure 2, the supply is margined to its high, low and nominal output voltages by driving the I/O pin to its high, low and high impedance states respectively. This example shows calculated resistor values rather than standard resistor values for ease of illustration. If the feedback voltage, V_{FB}, of the power supply is 0.8V, solve for the value of R_{FM1} that must be added in parallel with R_{F1} of the existing design to produce the desired high margin output.

In Figure 2, the feedback resistors R_{F2} and R_{F1} produce an output voltage of 2.5V. To margin 10% high to 2.75V requires a 54.4k resistor, R_{FM1}, in parallel with R_{F1}. Now connect a resistor, R_{TM1}, whose value is equal to R_{FM1} between the TRACK pin and ground. If the output will be margined low by the same voltage that it was margined high, then connect another resistor, R_{TM2}, equal to R_{FM1}, between the TRACK pin and the three-state I/O pin.

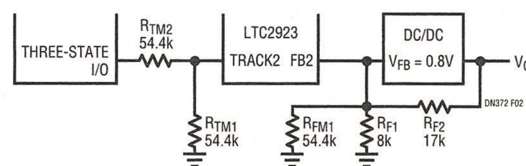

Figure 2. The LTC2923 Margins the Output of a 2.5V Supply 10% High or Low Under the Control of a Three-State I/O

In the circuit shown in Figure 3, an LTC2923 ramps up a 3.3V supply through a series FET, tracks a 2.5V supply to that 3.3V supply, and margins the 2.5V supply up and down by 10%. The first tracking cell connected to pins TRACK1 and FB1 causes the 2.5V supply to track this 3.3V supply during power up and power down as shown in Figure 4. The tracking cell connected to TRACK2 and FB2 is used to margin the 2.5V supply up and down by 10%.

The operation of the circuit in Figure 3 is simple. To margin high, the I/O pin is pulled above 1.6V. This pulls the TRACK2 pin above 0.8V so that no current is sourced into the feedback node of the power supply. The supply then defaults to its margined high output of 2.75V. For a nominal output, the I/O is high impedance. Now, no

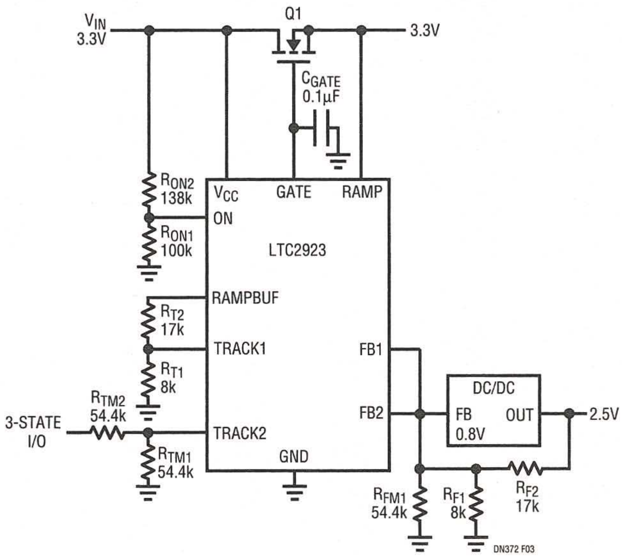

Figure 3. The 2.5V Supply Tracks the 3.3V Supply and Can be Margined High or Low by 10% Under Control of a Three-State I/O

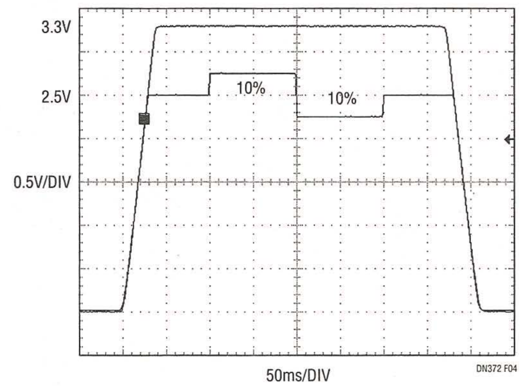

Figure 4. Output of Circuit in Figure 3. The 2.5V Supply Tracks the 3.3V Supply and is Margined High and Low by 10%

current flows through R_{TM2} but 14.7µA flows through R_{TM1} and is mirrored at the feedback node of the power supply. This forces the output voltage down by 250mV to 2.50V. For a margined low output, the I/O pin is pulled to ground. Now, 14.7µA flows through R_{TM2} in addition to the 14.7µA flowing through R_{TM1}. This current is mirrored at the power supply feedback node, and drives the output down by an extra 250mV from nominal.

Note that the ability to configure a current driven into the feedback node with R_{TM1} often allows the nominal output voltage to be closer to the ideal value than is possible with a single pair of standard value resistors, R_{F1} and R_{F2}, in the power supply feedback network.

If the desired high and low voltage margins, ΔV_{HIGH} and ΔV_{LOW}, are not equal simply adjust R_{TM2}. In this case, choose R_{FM1} as above to configure the high margin, and set $R_{TM1} = R_{FM1}$. Scale the voltage step ΔV_{LOW} relative to the voltage step ΔV_{HIGH} by choosing R_{TM2} by $R_{TM1}/R_{TM2} = \Delta V_{LOW}/\Delta V_{HIGH}$. For example, to change the margins in the above example to 10% high and 20% low, leave R_{FM1} and R_{TM1} unchanged at 54.4k, but reduce R_{TM2} is to 27.2k.

If the feedback voltage, V_{FB}, of the power supply is not 0.8V then the values of R_{TM1} and R_{TM2} are scaled by $0.8V/V_{FB}$. If the feedback voltage in the above example were 1.23V, then R_{TM1} and R_{TM2} would be scaled so that $R_{TM1} = R_{TM2} = R_{FM1} \bullet 0.8V/1.23V = 35.4k$.

Conclusion

The LTC2923's primary application is tracking power supplies, but its versatile architecture is suited to other functions as well. The application described here allows a three-state I/O to control supply margining using a few resistors and an LTC2923 tracking cell.

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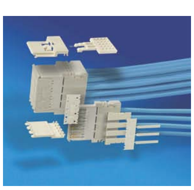

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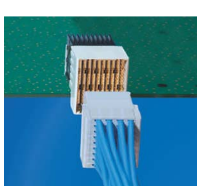

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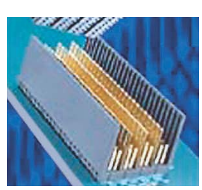

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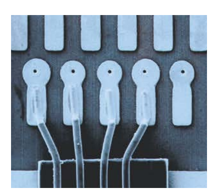

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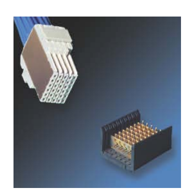

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Crystal resonators meet TPMS application requirements

Providing frequency control for transmitters or receivers in TPMS (tire-pressure-monitor-system) applications, the NX5032SD and NX8045GB crystal resonators meet tough shock, vibration drop, and acceleration requirements. The NX5032SD measures 5×3.2×1 mm and has a 9.84- to 40-MHz frequency range. The NX8045GB measures 8×4.5×1.8 mm and has a 5- to 40-MHz range and ±50-ppm frequency stability at 25°C. The NX5032SD and NX8045GB cost 55 and 43 cents (10,000), respectively.

NDK Co Ltd, www.paimarcom.com

Ceramic surface-mount crystal has extremely low profile

A new addition to the FX252B ceramic-surface-mount-crystal lines provides a 16- to 54-MHz frequency range, a ±50-ppm frequency tolerance, and a ±50-ppm frequency stability. With long-term gain of ±5 parts per billion per year, the device features a −10 to +60°C temperature range. The device is fully ROHS (reduction-of-hazardous-substances)-compliant and suits use in portable and space-constrained systems. The FX252B measures 2.5×2×0.6 mm and costs $2.86 (1000).

Fox Electronics, www.foxonline.com

All-quartz packaging has extremely low profile

Packaged completely in quartz crystal, the FQ5032 measures 5×3.2×0.8 mm. Available frequencies range from 12 to 50 MHz with a ±30-ppm tolerance at 25°C and standard stability of ±30 ppm at a 0 to 70°C temperature range. Suited for PDAs, MP3 players, scanners, and GPS equipment, the FQ5032 costs 25 cents (50,000).

Fox Electronics, www.foxonline.com

High-stability SAW oscillators have military-temperature range

The series I1050 SAW stabilized oscillators come in 1030- or 1090-MHz speeds. Operating at 12 dBm, ±2 dB with a stability of ±300 kHz, the oscillators have a temperature range of 55 to 105°C. Available as Jan- or Jantx-compliant, the product comes in an eight-pin hermetic DIP measuring 0.97×0.5×0.2 in. The I1050 series costs $85 (1000).

ILSI America, www.ilsiamerica.com

Operational amplifiers have extremely low noise and distortion

Low noise and distortion and a 1.1-mA supply-current draw highlight the ADA4841 family of single and dual devices for power-sensitive applications. The devices support 111 dBc and a 100-kHz SFDR (spurious-free dynamic range). Additional features include rail-to-rail outputs allowing a signal swing within 100 mV of either supply rail, 2.7 to 12V linear range for power supplies, a common-mode-voltage range extending to the negative supply for input, and a 500-µV offset voltage. Available in a six-pin SOT-23 and an eight-pin SOIC package, the ADA4841 costs $1.59 (1000), and the ADA4841-2 is available for sampling in eight-pin SOIC and MSOP packages for $2.29 (1000).

Analog Devices, www.analog.com

Wide-range amplifier has wide operating frequency

The LT5537 high-performance logarithmic detector features an operating-frequency range of near dc to 1 GHz and a measurement dynamic range of 90 dB. The device incorporates cascading chains of limiting amplifiers, providing a constant, linear 20-mV/dB logarithmic-detection function. The product also includes on-chip compensation circuitry to yield an accurate and stable output under varying temperature environments. It can measure signals within an error of ±1 dB. The LT5537 comes in a 3×2-mm DFN package and costs $2.95 (1000).

Linear Technology, www.linear.com

Single card has four functions

The FCAccess 4000 card operates as a Fibre Channel analyzer, a generator, an error injector, or a bit-error-rate tester. The multifunction card supports Fibre Channel transmission speeds of 1.062, 2.125, or 4.25 Gbps and all topologies or port types. As a Fibre Channel analyzer, the device captures and displays Fibre Channel traffic in an easy-to-read format and provides a true client/server, network-attached environment, allowing single or multiple users to employ it locally or remotely. Maximum trace memory is 4 Gbytes; cascading several analyzers can extend to larger recording space. As a Fibre Channel generator, the card operates in a host (initiator) or a target mode, allowing testing at the 8 or 10B level and providing low-level control of complex procedures, such as arbitrated loop initialization. As a Fibre Channel error injector, it introduces controlled error conditions into active Fibre Channel links without affecting traffic or data-link integrity. The FCAccess 4000 costs $14,200.

Ancot Corp, www.ancot.com

Embedded development environment supports MIPS architecture

Targeting MIPS32 and MIPS64 architectures, the Eclipse-based Nucleus Edge software-development environment includes a GUI providing demos and tutorials, allowing GUI interaction while the product is running. The software features an advanced project manager with an editor and a builder, allowing an automated building process after a designer specifies compilers and building options. It comes with the MIPS software-development-environment compiler. It costs $3000 per seat.

Accelerated Technology, www.acceleratedtechnology.com

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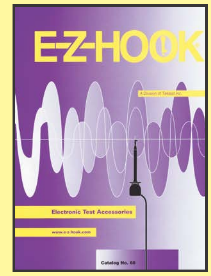

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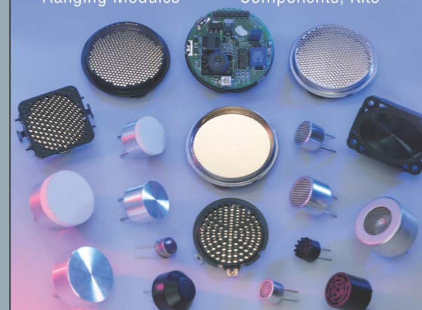

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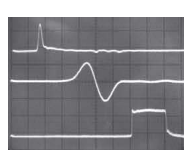

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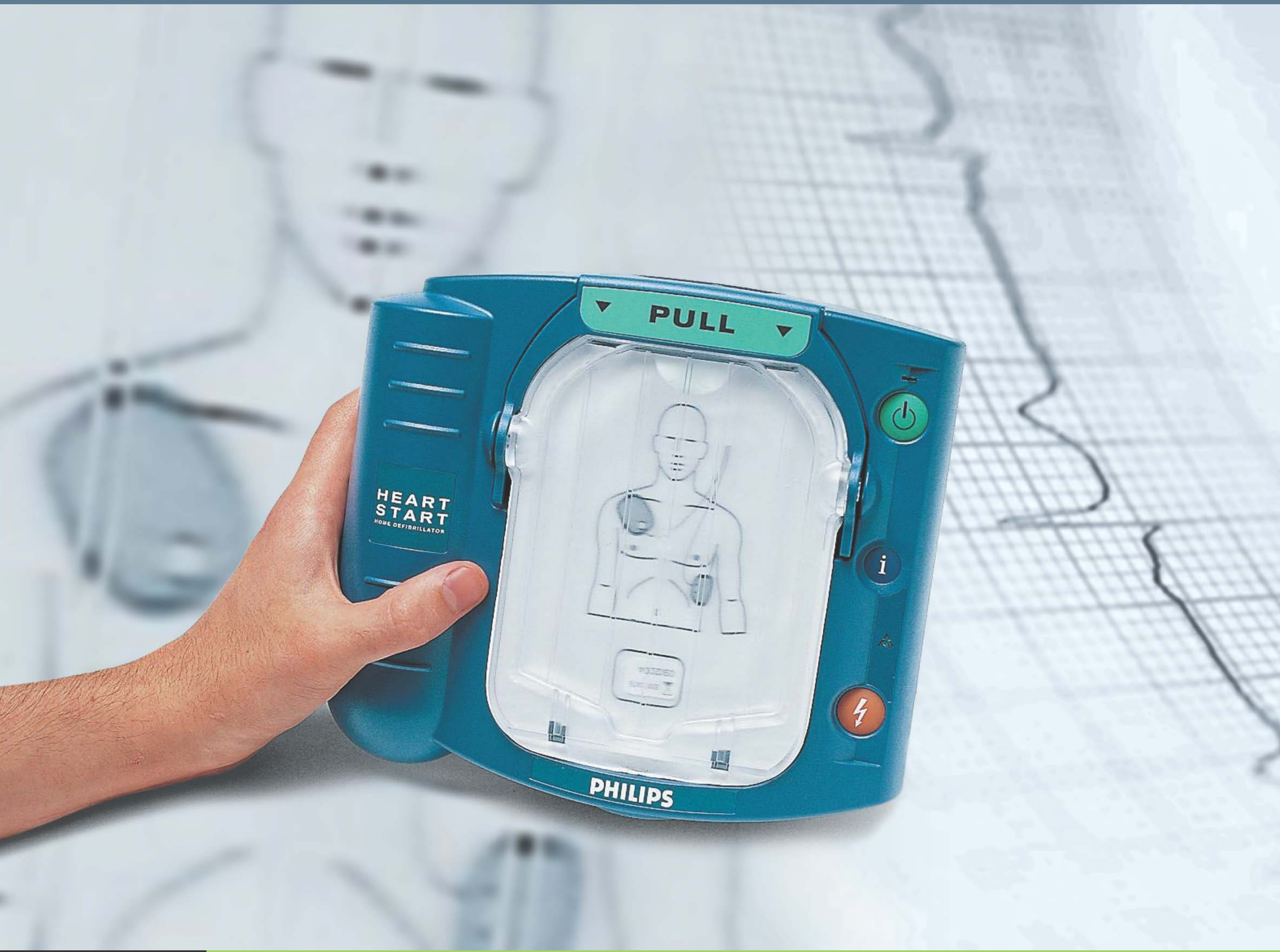

STATS More than 6000 sold since September 2004 / $1500 price tag

Home defibrillators give the market a new kind of shock

Until September 2004, when the Food and Drug Administration approved direct, online, and over-the-counter sales of defibrillators for home use, you could get a unit only with a doctor's prescription. Then, the HeartStart unit from the Philips Home Medical (www.heartstarthome.com) division of Koninlijke Philips Electronics NV received the requisite approval; thus far, this unit is the only one approved for such nonprescription home sales. Since that date, the company has sold more than 6000 of the $1500 units (see "Home defibrillator lets virtually anyone save a life," *EDN*, May 13, 2004, pg 27, www.edn.com/article/CA415111).

Although this number is small compared with the more than 100,000 prescription units sold in 2004 (with estimated revenue of about $300 million) to businesses, emergency medical technicians, and municipalities, it's a major wedge for selling sophisticated but easy-to-use medical electronics directly into the home. Other established medical-technology companies, such as Medtronic Inc (www.medtronic.com) are hoping to receive similar approval for home-market sales.—by Bill Schweber

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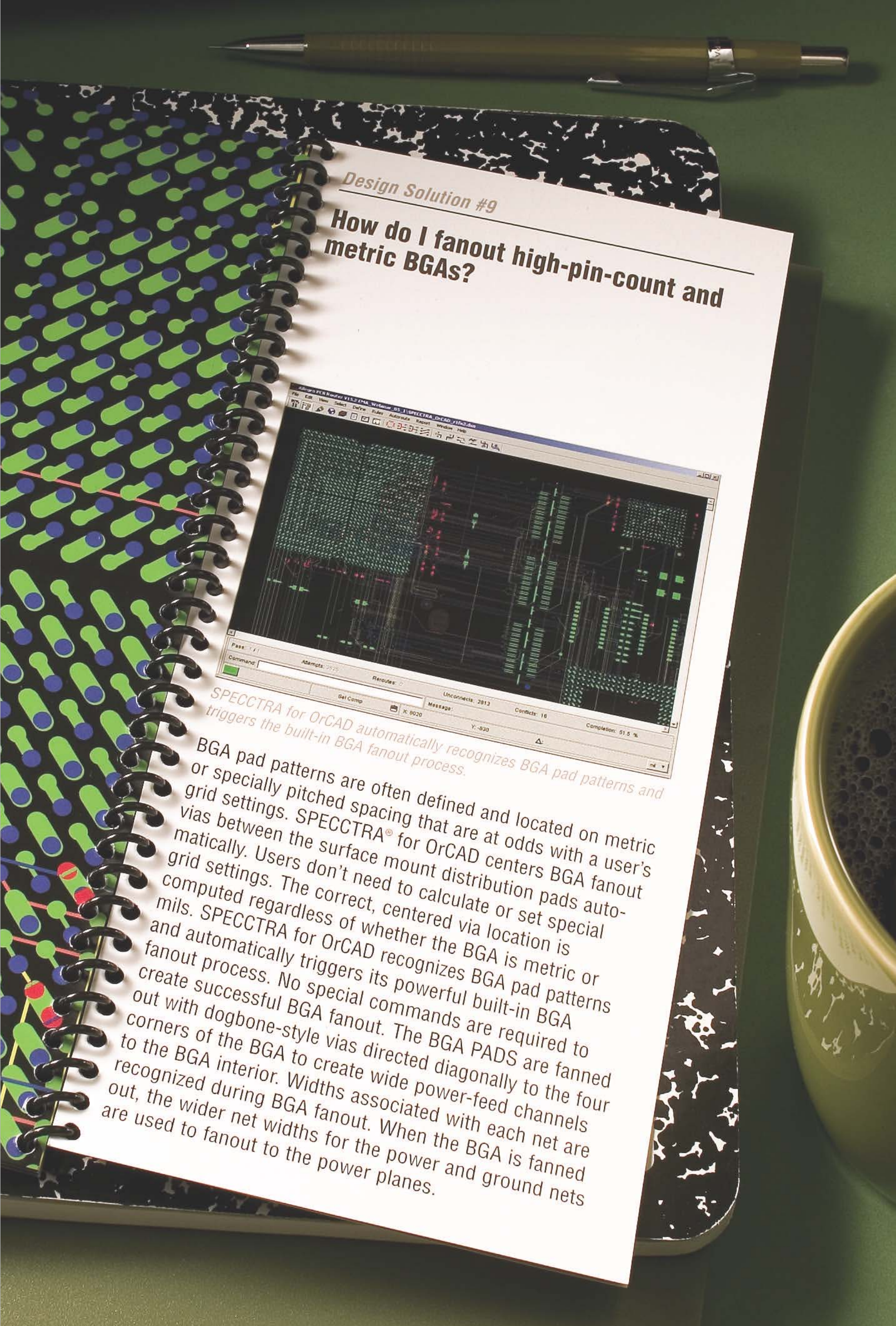

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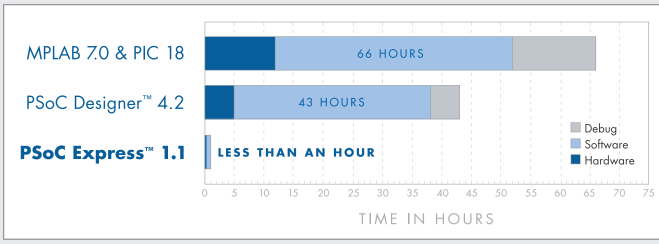

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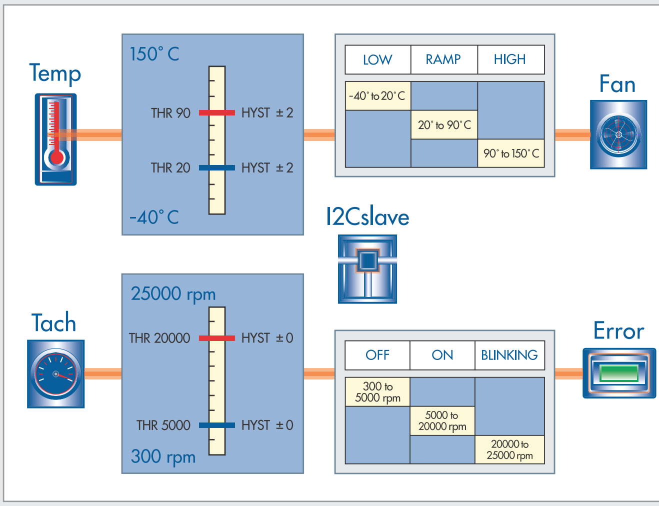

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